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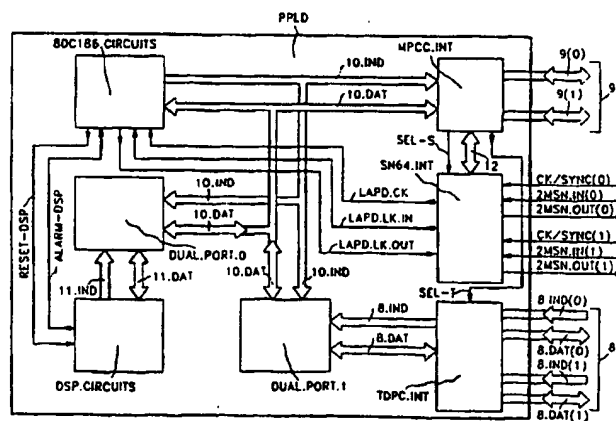
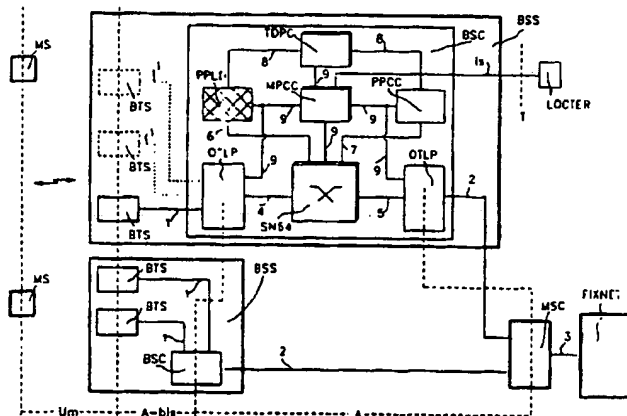
## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(54) Title: SIGNALING PROCESSOR FOR DIGITAL MOBILE RADIO SYSTEMS

## (57) Abstract

There is described a processor for signaling generated by transmission measurements included in a base radio station controller (BSC) of the pan-European mobile radio system (GSM®). The processor comprises a first microprocessor connected, through a dual access read and write memory, to a second microprocessor (DSP) and also interfaced with numerical signaling lines and a processor which manages the radio resources. The first microprocessor manages levels 1 and 2 of the signaling protocol LAPD and transfers to the DSP the level 3 messages which concern the transmission measurements of power and quality of the radio signal and of distance between the connected points. The DSP writes said messages in a dynamically managed RAM and at the same time processes the messages received to take back-messages comprising Handover decisions and indications for Power Control of mobile equipment.



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## SIGNALING PROCESSOR FOR DIGITAL MOBILE RADIO SYSTEMS

### DESCRIPTION

5           The present invention relates to mobile radio telephone systems and more particularly to a processor for telephone signaling generated by transmission measurements for digital mobile radio systems.

10           As is known, digital mobile radio systems differ from the analog type mainly in that they use transmission carriers modulated in accordance with numerical modulation techniques which are made necessary by the fact that the base band signal is already modulated digitally at the source. Digital mobile radio systems are now  
15           arising on the basis of more advanced concepts compared with those which inspired analog systems which make up the great majority of the systems now in use.

          It is also known that the telephone systems of the different countries conform to specifications issued in the form of recommendations by special supranational bodies (CEPT/CCITT) having  
20           the purpose of standardizing the operation of the different systems to make them mutually compatible and hence capable of communicating.

          The design of a modern mobile radio telephone system of the digital type is such a vast and ambitious project that it has required, at least in the European framework, cooperation of the  
25           principal managers of national networks and major manufacturers. Therefore, in 1983 in the framework of the European standardization agency CEPT there was created a special sub-group (ETSI) charged with preparing the specifications of a European digital mobile radio telephone system. At the present status, the phase of specification  
30           of a digital mobile radio system denominated GSM® has been completed and some prototypes are already going into service. For the sake of brevity the symbol ® will be omitted hereinafter.

          Since the non-limiting embodiment of the present invention relates to a particular application thereof within the pan-European  
35           digital mobile radio system GSM, some information of a general nature becomes necessary to explain said system. It is useful to recall that in extraEuropean areas, e.g. the United States and Japan, other

- 2 -

digital mobile radio systems are in operation but the GSM system is without doubt the more sophisticated and modern in conception. It is thus presently the most suitable to accommodate the present invention.

5           FIG. 1 shows a synthetic but explanatory block diagram of a GSM mobile radio system. In the figure the symbols MS (Mobile Station) designate mobile terminals, e.g. radio telephones mounted in motor vehicles, connected via radio with the respective transceivers TRX, not shown in the figures, belonging to one or more fixed radio  
10           stations indicated by the symbols BTS (Base Transceiver Station). Multiple BTS are connected to a base station (fixed) controller indicated by BSC (Base Station Controller), whose constituent blocks will be better explained below. The entirety collection of multiple BTSes governed by one BSC forms a functional sub-system indicated by  
15           BSS (Base Station System). Multiple BSC (BSS) are connected to an automatic telephone switching for mobile radio MSC (Mobile Switching Center) which is in turn connected to an automatic telephone switching of the fixed network FIXNET. At the MSC are located two data bases denominated HLR and VLR not shown in the figures. The  
20           former contains the permanent data of each MS while the second contains the variable data. The two bases cooperate in allowing the system to trace a user who makes broad movements in the territory. An Operation and Maintenance Center, also not shown in the figures, dialogues with MSC and BSC and carries out functions of supervision,  
25           alarm management, traffic measurement etc. termed E&M.

          The connection between a generic BTS with its own BSC, as between BSC and MSC, and between MSC and FIXNET, takes place over fixed numerical lines indicated by 1, 2 and 3 respectively. The figures show vertical broken lines delimiting the borders of the  
30           interfaces between the principal functional blocks and specifically Um indicates the radio interface between MS and BTS, A-bis that between BTS and BSC, A the interface between BSC and MSC, and T the RS232 interface between BSC and a local terminal LOCTER. The figures do not show the interface O provided between BSC and MSC. Said  
35           interfaces are described in GSM Recommendations 04.01 (Um), 08.51 (A-bis), 08.01 (A), 12.20 and 12.21 (O).

          The number of BTS, BSC and MSC blocks in FIG. 1 is only

- 3 -

indicative since in reality their actual number, like their location, is established in such a manner as to ensure uniformity of service all over the territory covered by the mobile radio service. For this purpose said territory is ideally divided in cells of appropriate  
5 size, each of which in case of central excitation is served by a BTS.

Every BTS comprises a group of transceivers TRX, one for each radio frequency carrier used in the cell. Every TRX is connected to a group of antennas whose configuration ensures uniform radio coverage of the cell. A group of N adjacent cells which together  
10 engage all of the carriers available to the mobile radio service is called a cluster. Said carriers can be reused in contiguous clusters. As set forth in GSM Recommendation 05.02 on multiple access to the radio path, the radio frequency band associated with a generic carrier is 200 kHz and is used with time division by 8  
15 different MS. The individual periods of use, approximately 0.577 ms, are termed 'time slots' and constitute the physical channels on which travels the information whether voice, data or signaling. Said information is divided in bursts consisting of appropriate bit sequences with each bit having a duration of approximately 3.69  $\mu$ s  
20 which occupy the respective time slots.

The group of 8 contiguous time slots constitutes a base frame lasting approximately 4.615 ms, repeated cyclically. The interface Um associates a logic channel with each physical channel and for this purpose multiple successive base frames are numbered and considered  
25 part of a repetitive multiframe. The meaning of the logic channel depends only on the position taken by the base frame in the multiframe in accordance with a diagram fixed by GSM Recommendations 05.01 and 05.02. If to the time slot is assigned a single logic channel the channel is termed full-rate. If to the time slot are  
30 assigned two logic channels with alternate frames, the two channels are termed half-rate.

The individual carriers used in a cell cluster are allocated contiguously in the radio frequency spectrum reserved for the GSM mobile radio service. Specifically, 124 carriers are possible for  
35 the sub-band reserved for uplink connection from MS to BTS (890 MHz to 915 MHz) and the same number for the downlink connection from BTS to MS (935 MHz to 960 MHz). The result is a maximum possible number

- 4 -

of 992 full-rate channels or 1984 half-rate channels.

The logic channels are distinguished in traffic channels called TCH which carry voice and data, and control channels which serve essentially for dialog between MS and BTS and carry signaling information and the values of some engineerable parameters.

Concerning voice channels TCH carried by the uplink connection time slot their generation starts from a digital modulation of the voice signal of the speaker. Said modulation produces a low bit-rate digital signal, typically 13kbit, as set forth in GSM Recommendations 06.01 and 06.10. The individual bits of the modulated voice signal are then manipulated in a complex manner to cipher and immunize to errors the transmitted information. Lastly, the bits are packaged in the bursts making up the TCH channels. Dual operations are completed on the voice reception signal bits of the TCH channel in the downlink connection.

As regards the control channels, there is provided a broadcast type control channel indicated by BCCH, a common control channel indicated by CCCH, and dedicated control channels indicated by DCCH.

The BCCH channel is a channel existing only in the downlink direction and serves to carry information on the cell type to the mobiles. It is unique for each cell and is broadcast from each BTS to all the listening MS only during the 0 time slot of a purpose-assigned carrier indicated by hereinafter BCCH carrier. The BCCH channel includes the subchannels FCCH and SCH consisting of homonymous bursts used by the mobiles to synchronize the frequency of its carrier and the frame of the digital channels with carrier and frame arriving from BTS respectively. The subchannel SCH comprises a field BSIC with the cell code number.

The channel CCCH is a two-way channel which serves the entire cell. It comprises a subchannel RACH in uplink direction with shared access which serves the entire cell and carries the access requests (random) of MS to the network, and two downlink subchannels AGCH and PCH which carry the responses of the network to the access requests and paging messages respectively.

The channels DCCH carry signaling and are divided in two categories of which the first comprises channels indicated by SDCCH which carry the signaling for control of the calls until assignment

of the channels TCH. A second category comprises channels indicated by SACCH which carry a signaling associated with the respective main channels, i.e. channels SDCCH or traffic channels TCH. They are therefore inserted in the same frame structure of said main channels.

5           The telephone signaling used in the framework of the GSM system makes use of the functions supported by a protocol with several hierarchical levels in large part taken from that presently in use in analog mobile radio systems or in land telephone systems. Level 1 of the above protocol indicates more specifically the type of physical  
10 carrier used for the connection. Level 2 develops functions which control the correct sequential flow of messages (transport functions) with the intention of providing a virtual carrier free of errors between the connected points. Level 3 (termed 'network') and the higher levels develop message processing functions for control of the  
15 main application processes.

          In the GSM mobile radio telephone system the mobile equipment MS carries out a certain activity even without a call. Indeed, as the first step to be able to communicate through the network, the mobile needs to be obliged to continuously choose a cell with which  
20 to associate while moving. This activity falls within the "Cell Selection and Reselection" function described in GSM Recommendations 03.22 and 05.08.

          The mobile chooses the cell with which to associate by completing a scanning of all the BCCH carriers provided by the GSM of which the MS has advance knowledge. For each of these it measures  
25 the power of the received signal, demodulates the RF signal, synchronizes with the multiframe structure of the demodulated signal to be able to acquire the cell code number and other useful information from the channel BCCH, and lastly updates a list of six  
30 most favoured cells. Among these, the preselected cell, also called 'serving' cell, is the one which results most reliable. The above operations are carried out periodically in the idle status, even when the mobile is already associated with a cell, in order to be able to reassociate with a different cell if it receives therefrom a BCCH  
35 carrier with better reliability (Cell Reselection). The mobiles which are synchronized with the frame of a BCCH carrier are also synchronized with the frames of the other carriers used in the cell

- 6 -

since the TRX of a BTS are all mutually synchronous. It follows that the frame number is unique within a cell.

The need of the MS to remain synchronized with the BTS with which they are associated does not end after association with a cell but reappears at every request for access thereof and persists throughout the conversation with BTS. A function termed 'Adaptive Frame Alignment' provides for this necessity, as set forth in GSM Recommendation 04.03, which allows the BTS to keep for a given channel three fixed advance time slots between the transmission and reception frames regardless of the movements of the mobile. In practice, when MS wants to accede to the network it sends to BTS an access burst which enables BTS to measure the actual delay and calculate a corresponding parameter termed 'timing advance' for the correction which MS must make in sending the subsequent frames on the uplink channel. At the end of the access phase a dialog is started between MS and BTS and the latter adjusts the timing advance continuously while calculating the subsequent delays of the uplink frames. The timing advance values are communicated by BTS to MS using a respective channel SACCH.

Access of MS to the network takes place in the following cases:

- by initiative of the user in originated call;
- by autonomous initiative of MS upon signaling of the network in paging call;
- by autonomous initiative of MS on signaling of the network in case of Handover (see below);
- by autonomous initiative of MS without intervention of user or network in case of particular functions, such as for example: affiliation, authentication, etc., which will not be discussed below.

In each of the cases mentioned MS sends an access burst on the control channel RACH or, in case of Handover, on the new assigned channel (SDCCH or TCH). Multiple requests can occur simultaneously but BTS solves the disputes. The MS which wins the dispute obtains from the network assignment of a free channel SDCCH on which a level 2 connection is established by activation in MS and BTS of the functions called for by the protocol termed LAPDm, as per GSM Recommendation 04.06. The level 3 messages for the services underway



can therefore flow. Said functions are activated for the traffic channel TCH which replaces the channel SDCCH.

5 Lastly there are illustrated two important functions of the GSM system, termed 'Power Control' and 'Handover', based on performance of special transmission measurements by the mobiles and BTS. Information on them is supplied in GSM Recommendation 05.08. Power Control and Handover, because of their importance, must continue to act even when a particular function termed 'Discontinuous Transmission' is activated and by which the mobile, and optionally 10 the BTS, are enabled for transmission of the carrier only if it is modulated, i.e. if there is vocal activity on the channels TCH. The purpose of this last function is to reduce the mean interference level in the network and at the same time increase the mobile operating range. The Handover function is typical of all mobile 15 radio systems and therefore it is provided, although in a less perfect manner, also in analog mobile radio systems. However, it does not seem that the latter carry out a function similar to that of Power Control of the GSM.

The transmission measurements performed by MS, in downlink 20 direction, concern the level and quality of the channels TCH and SDCCH in use, and the level of the BCCH carriers of the adjacent cells. These measurements generate values sent to BTS on the SACCH channels. Specifically, every MS which performs the measurements calculates a mean of the values measured extended to a SACCH 25 multiframe of 104 base frames, which corresponds to a time of approximately 480ms and the mean is inserted in the SACCH channel of the next multiframe.

The transmission measurements performed by BTS in uplink 30 direction concern the level and quality of the TCH and SDCCH channels in use, the value of the timing advance parameter, and the interference on the free time slots. Also in this case, for every MS to which the measurements are related, the measured values are averaged on the SACCH multiframe, the mean calculated by BTS is associated with that calculated by MS and the two means together are 35 sent to BSC through the interface A-bis to be used in the Power Control and Handover functions.

In case of 'Discontinuous Transmission' the measurements are

performed and averaged only on 12 of the 104 frames of the SACCH channel surely always present.

The Power Control function consists of the gradual change of power of a transmitter in steps of predetermined amplitude. The Power Control is governed by BSC and is performed obligatorily on the mobiles and optionally on the TRX. It takes place on all the time slots for the TCH traffic channels and SDCCH control channels independently for each individual channel and each individual MS. Excluded are the time slots of the BCCH carriers which carry control channels. Taking into consideration the Power Control activated on the mobiles, two cases are possible of which, in the first case transmitter power is decreased by steps of predetermined amplitude until it reaches a minimum level sufficient for the transmission conditions in the framework of the serving cell. In the second case power is increased by the same procedure until it reaches the maximum level deliverable by the transmitter. In the first case the purpose is to reduce the interference level on each channel, practically making activable very small cells also; secondarily the operating range of the mobile increases. In the second case the purpose is to avoid performance of Handovers for radio reasons when in reality they could be avoided.

The Handover function is to transfer on a free channel of good quality an on-going communication between an MS and a BTS on a channel (TCH or DCCH), which is released upon completion of the transfer. Handover is a basic function for any mobile radio telephone system because it is the function which allows the mobile to communicate while completing broad movements around the territory during the communication. Indeed, it prevents degradation of the transmission of the communication channel which otherwise would occur inevitably by way of the gradual moving away of the mobile from the complex of antennas of its initially serving cell. The preventive action must also be carried out without the user being able to perceive a disturbance on the on-going communication.

In the GSM system the Handover is started by BSC if the reason is faulty transmission quality on the channel in use. It is requested and governed by MSC if the reason is excessively intense traffic within a cell. And lastly it can also be requested by the

Operation and Maintenance Center for carrying out E&M functions. As regards the type of the Handovers, if they are performed between channels of the same cell they are termed 'intracell', but if they are performed between different cell channels they are termed

5 'intercell'. An intracell Handover involves an MS and a BTS and is usually governed by the BSC which has charge of the BTS. An intercell Handover involves an MS and two BTS and can be the internal or external type depending on whether the two BTS belong to a single or to two different BSC. In the first case the Handover can be

10 governed by the BSC while in the second case it must be governed by MSC.

Of the numerous and complex functions indispensable for operation of a mobile radio system of advanced conception, only those having the greater impact on the object of the present invention have

15 been mentioned until now. But it can already be inferred, and will appear more fully justified below, that the above functions require the support of powerful signaling managed by an adequate hardware and software structure. The processor of the telephone signaling originated by transmission measurements which are the object of the present invention confers on a digital mobile radio system in which

20 it can be used, e.g. the GSM system, the necessary requisites.

In mobile radio systems in accordance with the known art, essentially of the analog type, operation is governed by a specific configuration of processors wherein a first processor manages the

25 radio resources on the basis of the users' mobility, one or more second processors manage the lower signaling levels, and a third processor carries out maintenance and supervision functions. The above mentioned processors are generally microprocessors belonging to a controller of the fixed radio stations.

30 The above processors configuration, unless very costly processors are used, if it were translated into a digital mobile radio system of advanced conception, could not ensure optimal management of the signaling originated by the transmission measurements. This is basically due to the fact that in modern

35 digital systems, telephone signaling between mobile equipment and the fixed radio station control equipment is very much more intense and sophisticated compared with that used in known mobile radio systems.

- 10 -

The additional signaling is on the whole originated by the more extended control performed on the mobile equipment and on the transceivers of the fixed radio stations, mainly as concerns adjustment of the power of the transmitters and performance of better  
5 Handovers. In the GSM system, for example, the only signaling originated by the transmission measurements generates two level-3 messages per second for each traffic channel, whose processing also requires performance of a considerable number of arithmetic operations.

10 In view of the foregoing, using the processor configuration of the known art in a controller of the fixed radio stations of a digital mobile radio system of advanced conception, the real time available to the processor dedicated to radio resource management would be quickly saturated, because in this case it would also have  
15 to take on the additional processing load generated by the transmission measurements. However it is not expedient to transfer this processing to a processor dedicated to management of the lower levels of signaling because the latter, because of the very nature of their task, is already absorbed by pressing real time problems.  
20 Accordingly, the above remarks on the basic inadequacy of the known processor configuration appear justified.

It can be readily understood how vital it is for a mobile radio system to have a very efficient hardware and software structure for management of the signaling generated by transmission measurements,  
25 since it is exactly from said processing that descends the possibility of equipping the mobile radio system with specific functions designed to make it of advanced conception.

The required efficiency means mainly high computing speed and processing capability able to face intense telephone traffic without  
30 creating long waiting queues and all this while using economical hardware.

The present invention satisfies these requirements, having for its object a processor of telephone signaling generated by transmission measurements as described by the entirety of the claims.

35 The processor of the telephone signaling generated by transmission measurements which is the object of the present invention belongs to a control unit for multiple fixed radio stations

- 11 -

of a digital mobile radio telephone system. Said control unit also comprises a telephone processor dedicated to the management of radio resources on the basis of the users' mobility, and an administrative processor which carries out maintenance and supervision functions, and it is connected by means of first and second numerical lines carrying voice, data and signaling channels to fixed radio stations and to an automatic telephone switch for mobile radio systems respectively.

Said telephone signaling processor consists substantially of a first processing unit, based on the use of a general-purpose microprocessor, which communicates with a second processing unit, based on the use of a microprocessor specialized in the performance of arithmetic operations in real time, through a dual-access RAM. The first processing unit is also connected to the telephone and administrative processors and to the first numerical lines by means of respective interfaces.

The first processing unit manages the lower levels of signaling existing on the first numerical lines to allow flow of high-level messages in both transmission directions, among which it selects those generated by transmission measurements and writes the information content thereof in the dual-access RAM and sends, by means of said interfaces, the messages which do not concern transmission measurements to corresponding destination members.

The second processing unit reads from the dual-access RAM the information content written by the first processing unit and writes it in the areas of its own memory dynamically assigned to the channels, then it processes appropriately said contents to obtain further messages comprising indications and commands for performance of the Handovers and for control of the power of the transmitters included in the mobile units, and optionally fixed units, and writes said further messages in the dual-access RAM.

The first processing unit reads from the dual-access RAM the messages written by the second processing unit and adds thereto control fields to obtain complete messages which it sends, through the above interfaces, to the fixed radio stations and mobile units for performance of Power Control and Handovers.

A mobile radio system possessing a processing unit purposely

- 12 -

dedicated only to transmission measurements has undoubted advantages compared with known systems.

A first advantage is that, although faced with the new and more burdensome processing requirements, the work load is substantially  
5 balanced between the different processors; consequently the telephone processor which manages radio resources dedicated to users can handle more intense telephone traffic.

A second advantage, substantially due to the use of a mathematical microprocessor, is that of being able to monitor in real  
10 time the actual operating conditions, from the transmission viewpoint, of the mobile and fixed units, in order to be able to optimize said conditions. Specifically: the power of the transmitters of the fixed and mobile units can be systematically regulated in such a manner that it is adequate for the transmission  
15 situation, thus making feasible very small cells where the telephone traffic is most intense; the Handovers can be decided on a much broader data base and this allows Handover decisions more responsive to the requirement to extend in time the good quality of the voice channels and reliability of the data channels.

A third advantage is due to the fact that the memory included  
20 in the second processing unit is managed in such a manner as to obviate the limitations generally possessed in this task by mathematical microprocessors. In particular, dynamic management thereof allows the use of a small RAM to meet the necessities  
25 deriving from intense telephone traffic.

The foregoing remarks together with the fact that the two processing unit comprise low-cost microprocessors easy to find, involves a low overall cost of the processor in question.

Additional purposes and advantages of the present invention  
30 will be clarified by the following detailed description of an embodiment thereof given by way of non-limiting example in which:

FIG. 1 shows a very general block diagram of a mobile radio system of the GSM type;

FIG. 2 shows a more detailed diagram of a block, indicated by  
35 PPLD in FIG. 1, representing the processor of telephone signaling originated by transmission measurements which is the object of the present invention;

FIG. 3 shows a more detailed block diagram indicated by DSP.CIRCUITS in FIG. 2 and representing a processing unit dedicated to the level 3 messages originated by said transmission measurements;

FIG. 4 shows a block diagram of the governing program of another processing unit dedicated to level 2 messages and represented by a block indicated by 80C186.CIRCUITS in FIG. 2;

FIG. 5 shows messages processed by the unit DSP.CIRCUITS of FIG. 3;

FIGS. 6a and 6b show the main fields included in a message of FIG. 5;

FIG. 7 shows a table structure used by the processing unit DSP.CIRCUITS to address dynamically a memory indicated by the symbol RAM in FIG. 3;

FIG. 8 shows the image of the partial content of said RAM of FIG. 3, and

FIGS. 9 to 15 show the flow charts for the program governing operation of the processing unit DSP.CIRCUITS of FIG. 3.

With further reference to FIG. 1 it can be noted that the controller of the base station BSC comprises two identical blocks indicated by OTLP, a block SN64, a block PPLD, a block TDPC, a block MPCC, and lastly a block PPCC. A first of the two blocks OTLP is connected to multiple BTS by means of the lines 1 and to the block SN64 by means of other two-way numerical lines 4. A second block OTLP is also connected to the block SN64 by means of two-way numerical lines 5 and to the block MSC through the lines 2. The block SN64 is also further connected to the blocks PPLD and PPCC by means of two other numerical lines indicated by 6 and 7 respectively. Each of the lines 4, 5, 6 and 7 consists in reality of a one-way line for each transmission direction. The block TDPC is connected to the blocks PPLD and PPCC by means of a bus 8. The block MPCC is connected to all the blocks of BSC by means of bus 9 and to the terminal LOCTER by means of a serial data line 1s. In the figures, for the sake of brevity, there is not shown a block comprising a high-stability oscillator generating a clock signal from which are derived all the timings used by the BSC blocks.

For reasons of reliability the blocks MPCC, TDPC, SN64 and clock are duplicate and consequently the busses 8 and 9 are duplicate

busses just as the numerical lines 4, 5, 6 and 7 are duplicate.

The lines 1 are one-way lines in both transmission directions which carry serial numerical flows conforming to interface A-bis. Said flows are of PCM type with 2048 kbit/s, in conformity with CCITT G. 703, and comprise 64 kbit/s traffic and signaling channels. The signaling is based on protocol LAPD (Link Access Procedure on the D-channel) as per CCITT Recommendations Q920, Q921. A signaling channel LAPD, termed also 'channel D', is associated with a preset number of traffic channels, maximum 30 full rate. In the GSM system there is also provided the possibility of replacing a 64 kbit/s signaling channel LAPD with one or more 16 kbit/s channels. The operation of conversion from interface Um to A-bis and vice versa is completed mainly by the BTS, which involves conversion of the voice channels TCH in time slot PCM to 8 bit and conversion of the signaling protocols from LAPDm to LAPD.

The lines 2 are one-way lines in both transmission directions which carry serial numerical flows conforming to interface A. Said flows are also of PCM type at 2048 kbit/s CCITT G. 703, but comprising 64 kbit/s signaling channels of the Common Channel CCITT No. 7 type.

One of the signaling channels is used to implement the O interface based on protocol CCITT X.25 provided between the Operation and Maintenance Center and BSC. Conversion between the interfaces A-bis and A and vice versa is completed by the BSC.

Below is given some information on the constitution and operation of the blocks MPCC, PPCC, TDPC, OTLP and SN64 to make more comprehensible the present invention substantially included in the block PPLD which will be discussed more thoroughly below.

The block MPCC shows an administrative processor which controls and supervises the entire operation of the BSC and as such has a standard double interface toward all the blocks of BSC considered as peripherals and to which it is connected by means of duplicate busses for addresses, data and control signals and indicated by 9 in FIG. 1. The two copies of MPCC work in active/hot-standby configuration and in each block MPCC is included a circuit which implements the configuration and control logic of the BSC as concerns redundancy. Said circuit generates the copy selection signals used by the



peripheral blocks to select the bus 9 of the active copy to which to connect.

The block PPCC is a peripheral processor which manages levels 1 and 2 of the CCITT No. 7 signaling used at interface A.

5       The block TDPC shows a telephone processor which manages the application processes for control of the calls, administrating the radio resources on the basis of user mobility. It also has the task of exchanging messages between the two peripheral signaling processors PPLD and PPCC, which implies conversion of the exchanged  
10       messages between protocols LAPD and CCITT No. 7.

      The two identical blocks OTLP constitute line terminations for the 2048 kbit/s PCM lines 1 and 2 and supply the interface between these lines and a duplicate switching network represented by the block SN64. As such, the two blocks OTLP carry out all the functions  
15       which a normal known termination must carry out; i.e. equalization of the arriving signal from which is extracted a clock signal optionally usable for timing the various circuits, conversion of the line codes, preparation of an elastic memory to compensate the line delays and for plesiochronous operation, detection of on-line alarm conditions,  
20       extraction of frame synchronisms, etc.; there is also included the function of extraction/insertion of the 64 kbit/s signaling channel from/to the Operation and Maintenance Center. Each block OTLP possesses a line controller which interfaces with the administrative processor MPCC with which it cooperates for supervision and  
25       maintenance operations.

      The switching network SN64 supplies the two-way connections between the traffic channels at 16 kbit/s or 64 kbit/s which are present on lines 1 and 2. It is required, because said channels are distributed differently between the two line groups, the lines 2 are  
30       generally fitted out in a smaller number because they are longer and costlier, hence more densely utilized.

      Another important function of the network SN64 is to provide the semi-permanent (nailed up) connections for the signaling channels to the peripheral processors PPLD and PPCC. For this purpose the  
35       signaling time slots LAPD which travel on the lines 4 toward SN64 are extracted and inserted in 2 Mbit/s serial numerical flows consisting of only signaling channels carried by the lines 6 to PPLD.

- 16 -

Reciprocally, the signaling channels LAPD generated by PPLD constitute the time slots of 2 Mbit/s numerical serial flows of signaling channels carried by the lines 6 to SN64. Fully equivalent operations take place as regards sorting of the CCITT No. 7 signaling channels from the lines 5 to PPCC and vice versa through the lines 7.

The terminal LOCTER is a personal computer which dialogues with MPCC and provides the man/machine interface for starting of operations such as for example: initialization, software loading, diagnosing, etc.

The diagramming of the controller BSC of FIG. 1 being general in nature it does not relate to an actual on-site installation case. Therefore, since each block BSC is implemented in one or more boards, the quantity of the different boards is not given. As concerns the number of boards for the blocks MPCC, TDPC, SN64 and clock generator, it is constant for the BSC. While as concerns the number of boards for the blocks OTLP, PPLD and PPCC it will be determined upon each new installation on the basis of the telephone traffic expected for the mobile radio service in the area served by the BSC. Said number is also redounded by one unit for reliability reasons.

With reference to FIG. 2, in which the same elements of FIG. 1 are indicated by the same symbols, there is described block PPLD which includes the object of the present invention.

In FIG. 2 can be seen a first processing unit 80C186.CIRCUITS connected by means of two busses 10.IND and 10.DAT to first gates of two dual-access RAM DUAL.PORT.0 and DUAL.PORT.1 and to an interface circuit MPCC.INT to the two copies of the administrative processor MPCC of FIG. 1. A second processing unit DSP.CIRCUITS is connected by means of two busses 11.IND and 11.DAT to a second gate of the memory DUAL.PORT.0. An interface circuit TDPC.INT to the duplicate telephone processor TDPC of FIG. 1 is connected, by means of two busses 8.IND and 8.DAT, to a second gate of the memory DUAL.PORT.1.

The interface MPCC.INT is also connected by means of two busses 9(0) and 9(1), corresponding to the busses 9 of FIG. 1, to two respective copies of MPCC. Similarly the interface TDPC.INT is also connected by means of two pairs of busses 8.DAT(0), 8.IND(0) and 8.DAT(1), 8.IND(1) respectively, corresponding to the busses 8 of FIG. 1, to two respective copies of TDPC.

- 17 -

The unit 80C186.CIRCUITS is also connected to an interface circuit SN64.INT towards the duplicate switching network SN64 of FIG. 1 by means of the numerical lines 6 (FIG. 1). Specifically, from each copy of the network SN64 arrives at SN64.INT one or more

5 2 Mbit/s serial numerical flows (made up only of time slots LAPD) indicated by 2MSN.IN(0) and 2MSN.IN(1) respectively and each flow being associated with a timing indicated by CK/SYNC(0) and CK/SYNC(1) respectively. From the circuit SN64.INT emerges a plurality of 16/64 kbit/s LAPD numerical serial signaling flows indicated by LAPD.LK.IN

10 and accompanied by a plurality of clock signals LAPD.CK. Said plurality is directed to the processing unit 80C186.CIRCUITS. Similarly, from the unit 80C186.CIRCUITS emerges a plurality of as many 16/64 kbit/s LAPD numerical serial signaling flows indicated by LAPD.LK.OUT directed to the circuit SN64.INT where it originates one

15 or more pairs of 2 Mbit/s serial numerical flows (made up of only LAPD time slots) indicated by 2MSN.OUT(0) and 2MSN.OUT(1) and directed to the two copies of the network SN64 respectively.

Specifically, each flow 2MSN.IN(0) or 2MSN.IN(1) carries 8 LAPD time slots to the PPLD board, the remaining time slots being

20 available for other PPLD boards optionally fitted out. A signaling channel LAPD remains identified in both transmission directions by the identical position which the related time slot takes in the flows 2MSN.IN(0), 2MSN.OUT(0) or 2MSN.IN(1), 2MSN.OUT(1).

The interface circuit SN64.INT is also connected to MPCC.INT by

25 a two-way bus indicated by 12.

From the interface circuit MPCC.INT depart two selection signals SEL-S and SEL-T directed to the interface circuits SN64.INT and TDPC.INT respectively.

The two processing units 80C186.CIRCUITS and DSP.CIRCUITS

30 exchange two signals denominated RESET-DSP and ALARM-DSP, whose meaning is explained below.

The explanation of the operation of the individual PPLD blocks, as regards the purely circuit point of view, is given without the aid of detailed drawings of the individual circuits included therein with

35 the exception of those belonging to the block DSP.CIRCUITS. The following considerations on the circuit constitution thereof together with what is published in the technical sheets accompanying the

various devices used, to which reference is made, are sufficient for those skilled in the art to obtain the constitutive hardware of said blocks. It is specified that the list of the circuits referring to a block is not always physically present in said block. Indeed, a good  
5 part of the hardware constituting the PPLD is obtained by means of a gate array designed purposely.

The unit 80C186.CIRCUITS comprises the following circuits and devices:

- 10 - an Intel 80C186XL-20 microprocessor indicated hereinafter by 80C186 and characterized by having a 20-line bus on which it multiplexes the addresses and data and with which are associated further lines for the appropriate control signals for the operations on the bus. The data consist of 16-bit words transferable wholly in a single operation (in word mode) or by means of two distinct operations (in  
15 byte mode) in which the two bytes making up each individual word are individually addressable;
- latches which hold steady for the entire duration of a bus cycle the address signals generated by the microprocessor making them separately available on the bus 10.IND;
- 20 - transceivers which are enabled selectively by the read and write control signals generated by the microprocessor for setting the correct input or output direction of the data on the bus 10.DAT;
- an EPROM in which is memorized the firmware concerning the basic operation of the 80C186;
- 25 - a static RAM of ample size in which is loaded the application software physically divided in two banks with which is associated another bank reserved for the parity bits. The two banks are respectively designed for the lower and upper bytes of the bus 10.DAT;
- 30 - serial communication controllers SAB 82525 termed hereinafter HSCX;
- a selection circuit (chip select) connected to the bus 10.IND which decodes for each read and write operation in memory or input/output the address configuration present on the bus 10.IND and generates therefor a respective enablement signal for a device or circuit  
35 belonging to the unit or to the other PPLD blocks reached through its buses;
- a circuit generating one or more parity bits of the data during the

write operations performed by the microprocessor, said bits having purposeful dedicated lines on the bus 10.DAT, and which check parity during the read operations, generating an alarm signal in case of parity error;

- 5     - a register in which is memorized the above alarm and the address present at that time on the bus 10.IND;
- a logic circuit which in case of alarm for parity error generates an interrupt toward the 80C186 causing inhibition by the software of the write operations addressed to the DUAL.PORT.0 or to the
- 10    DUAL.PART.1 or to a group of communication registers with MPCC located in the block MPCC.INT until the alarm is removed;
- a register in which is memorized a parity error alarm coming from DSP.CIRCUITS;
- a register in which is written a bit used as a control point for
- 15    reset of a microprocessor inside the unit DSP.CIRCUITS; and
- additional devices which aid the microprocessor in some particular operations as for example management of direct memory access (DMA) and interrupt.

20     All the above listed circuits and devices making up the unit 80C186.CIRCUITS are connected to the busses 10.IND and 10.DAT; with said busses are also associated the lines for the control signals generated by the microprocessor, for those of interrupt and for said enablement signals.

25     Each serial communications controller HSCX is assigned to a serial numerical flow LAPD. Specifically, the serial reception part of HSCX receives a flow LAPD.LK.IN and the serial transmission part transmits a flow LAPD.LK.OUT. The speed of the serial communication is set by MPCC independently for each HSCX, because 16 kbit/s LAPD numerical flows are also possible. The HSCX have

30    reception/transmission buffers for transfer of data to/from the processing unit RAM, which takes place on the basis of interrupts sent by the HSCX to the 80C186.

35     The microprocessor 80C186 can address 1Mbyte of physical memory for normal read/write operations and possesses another addressable 64kbyte space reserved for input/output operations. Its addressing space is shared among all the devices and circuits to which it has access through its busses and this applies also for sharing of the

space reserved for input/output operations. Operation of the 80C186 is timed by a 40MHz clock signal taken locally.

The blocks DUAL.PORT.0 and DUAL.PORT.1 are two identical static dual-access RAM having 16-bit words plus two bits of parity. These  
5 are provided by commonly available integrated circuits. Each memory possesses two access gates to which are connected the busses of two different processors respectively. The above memories are partitionable in areas in which read and write accesses are disciplined by respective one-bit registers, called hereinafter  
10 semaphores, programmable independently from each other. The programming consists of engagement of the semaphore to be able to accede to the memory area associated with it or to release of the semaphore after completion of the access. Semaphorized management of the dual-access RAM in practice makes possible two simultaneous  
15 accesses by two processors, provided said accesses are for two different memory areas. The dual-access memory chips have inputs for respective enablement signals.

The circuit configuration of MPCC.INT is in large part like that of two identical interface circuits used by the duplicate  
20 processor MPCC to implement the standard double interface toward the peripheral blocks reached by the busses 9 of FIG. 1. Incidentally each of said peripheral blocks must therefore include an interface circuit of the MPCC.INT type. The bus 9 comprises eight lines on which the active processor MPCC multiplexes the addresses and data  
25 and a ninth line for a parity bit added to the data. In addition, the bus 9 being the only connection indicated in FIG. 1 between MPCC and the peripheral blocks, it must necessarily comprise the lines reserved for the control, interrupt, copy selection, board enablement, etc. signals.

30 The interface circuit MPCC.INT comprises the following circuits:

- of the transceivers connected to the buses 9(0) and 9(1);
- a selection circuit to whose inputs arrive copy selection signals from both the interface circuits included in the duplicate block  
35 MPCC. The selection circuit generates a signal which enables only the transceivers connected to the bus 9 which leads to the interface used by the active MPCC copy and said bus is thus

extended in PPLD;

- circuits which control the parity of data and addresses of the active bus 9 and, in case of parity error, generate respective alarm signals;
- 5    - an alarm register in which are memorized said alarms;
- a logic circuit which in case of parity error alarm on the active bus 9 generates an interrupt toward MPCC causing reading of the related alarm register by MPCC and inhibition of its possible write cycles toward MPCC.INT until the alarm register is zeroed;
- 10   - a first group of registers comprising: registers in which is memorized the recapitulatory situation of the PPLD alarms to which MPCC can accede in reading; status registers in which MPCC writes software control points, corresponding to the signals SEL-S and SEL-T; registers in which the microprocessor 80C186 writes software
- 15   control points to force an alarm condition in the different PPLD alarm registers to verify correct operation of the circuits generating and verifying said alarms; registers in which the 80C186 writes other software control points to force circuit
- 20   configurations different from those of normal operation in order, for example, to verify the integrity of the path of a generic LAPD channel; or to start other operations provided for circuit maintenance;
- a second group of registers in which MPCC writes the position of the time slots of the flows 2MSN.IN to be assigned to respective
- 25   channels LAPD.LK.IN; the same position applies also for the time slots of the 2MSN.OUT flows in which are inserted the corresponding channels LAPD.LK.OUT; also included are registers in which MPCC writes two speed values, 16kbit or 64kbit per sec, of each LAPD flow;
- 30   - a third group of registers comprising communication registers between the microprocessor 80C186 of PPLD and the processor MPCC; the registers of the third group are 8-bit registers connected together and to the busses 10.IND, 10.DAT and active 9, in such a manner as to allow a dual read and write access by both the
- 35   processors; for this purpose, to said registers reach appropriate timings taken from the control signals coming from the processing unit 80C186.CIRCUITS and from the processor MPCC, with the purpose

of making the busses 10.IND, 10.DAT and active 9 congruent. Some of the registers of the third group are also used as semaphores to discipline access to the communication registers, similarly to what takes place inside the DUAL.PORT.0 and DUAL.PORT.1 memories;

- 5   - a selection circuit (chip select) connected to the active bus 9 which decodes the address configuration and generates enablement signals directed to the registers of the three different groups and to the semaphores associated with the registers of the third group respectively.

10       The interface circuit TDPC.INT comprises the following circuits:

- of the transceivers connected to the busses 8.DAT(0) and 8.DAT(1);
- of the selectors connected to the busses 8.IND(0) and 8.IND(1);
- a logic circuit to which arrives the signal SEL-T for enablement of only the transceivers connected to the bus 8.DAT which leads to the active copy TDPC; said bus is then extended into the PPLD; the signal SEL-T also reaches the selection input of said selectors of the address busses to determine the choice of the active bus 8.IND, which is also extended into the PPLD;
- 15   - of the circuits which at each bus cycle verify the parity of data and addresses of the active bus 8 and, in case of parity error, generate an alarm signal;
- 20   - of the registers in which are memorized said alarms;
- a logic circuit which in case of alarm generates an interrupt to TDPC, causing reading of the alarm registers by the latter and inhibition of its possible write cycles in the DUAL.PORT.1 until the alarm registers are zeroed;
- 25   - a selection circuit (chip select) connected to the bus 8.IND which decodes the address configuration and generates for the enablement signals directed to the alarm registers, to the memory DUAL.PORT.1, and to its assigned semaphores.
- 30

The interface circuit SN64.INT comprises two-input selectors to which arrive respectively:

- the timing signals CK/SYNC(0) and CK/SYNC(1);
- 35   - the numerical flows 2MSN.IN(0) and 2MSN.IN(1);
- two first numerical parity flows (not shown in FIG. 2) associated with the flows 2MSN.IN(0) and 2MSN.IN(1);



- 23 -

- the numerical flows 2MSN.OUT(0) and 2MSN.OUT(1);
- two second numerical parity flows (not shown in FIG. 2) associated with the flows 2MSN.OUT(0) and 2MSN.OUT(1).

At the selection input of each selector arrives the signal  
5 SEL-S which selects at output the numerical flows from, or directed to, the active copy of the switching network SN64 of FIG. 1. Said selected flows are also indicated for convenience by 2MSN.IN, 2MSN.OUT and CK/SYNC. The timing signals CK/SYNC comprise 8 MHz  
10 clock signals CK, from which are taken 2 MHz signals, and related 8 kHz signals SYNC which designate the frame start of the numerical flows 2MSN.IN and 2MSN.OUT.

The circuit SN64.INT also comprises:

- a synchronism generator to whose inputs arrive the timings CK/SYNC and, by bus 12, the output configurations of the MPCC.INT registers  
15 belonging to the second group. Said generator generates at its outputs the following signals: synchronism signals for extraction of the time slots from the 2 Mbit/s flows, and dually for the related insertion; synchronism signals for generation and verification of parity on the parity flows; and the plurality of  
20 16/64 kbit/s clock signals indicated by LAPD.CK;
- a time slot extraction circuit generating at output the pluralities of numerical flows LAPD.LK.IN to whose inputs arrive the flows 2MSN.IN, the timings CK/SYNC and the signals output from the synchronism generator;
- 25 - a time slot insertion circuit generating at output the flows 2MSN.OUT to whose inputs arrive the pluralities of numerical flows LAPD.LK.OUT, the timings CK/SYNC, and all the signals output from the synchronism generator;
- a circuit which verifies the parity of the flows 2MSN.IN and  
30 generates an alarm every time it finds a parity alarm and to whose inputs arrive said flows 2MSN.IN, the respective first numerical parity flows, the timings CK/SYNC, and said synchronisms for parity verification;
- a circuit generating second numerical parity flows associated with  
35 the flows 2MSN.OUT to whose inputs arrive said flows 2MSN.OUT, the timings CK/SYNC and said synchronisms for parity generation;
- a circuit verifying the integrity of the paths of the LAPD channels

comprising two groups of two-way electronic switches to which arrives, by the bus 12, a respective command (control point) from 80C186. The first group of switches serves to verify the path taken by a generic LAPD channel predominantly in the network SN64 of FIG. 1 and the interface SN64.INT. For this purpose the line carrying the channel LAPD.LK.IN preselected is switched onto that carrying the corresponding channel LAPD.LK.OUT avoiding the microprocessor 80C186; after which the network SN64 sends a known pattern on the flow 2MSN.IN and verifies correct reception of said pattern on the flow 2MSN.OUT. The second group of switches serves to verify the path taken by a generic channel LAPD predominantly within PPLD. For this purpose the line carrying the flow LAPD.LK.OUT comprising a preselected LAPD channel is switched onto that carrying the corresponding flow LAPD.LK.IN avoiding the path inside the network SN64; after which the microprocessor 80C186 sends a known pattern on the channel LAPD.LK.OUT and verifies the correct reception of the pattern on the channel LAPD.LK.IN.

The synchronism generator comprises substantially first and second counters and digital comparators. The extraction circuits and time slot insertion circuits comprise substantially shift registers with parallel loading. The parity verification and generation circuits are obtained with purposeful integrated circuits easy to find.

The synchronism generator in its operation uses said first counters for generation of the 16/64 kHz clock signals LAPD.CK. For this purpose the signals SYNC start counting the rising edges of the signals CK and the outputs of the counters corresponding to division by 32/128 are used to generate the signals LAPD.CK. The second counters are increased by the edges of the signals LAPD.CK and at each increase their output configuration is compared with the respective content of said second registers of MPCC.INT and the cases of coincidence originate the extraction/insertion synchronisms corresponding to active signals for the entire duration of the respective time slots. The parity synchronisms are pulses which mark the start of each time slot and are taken from the timings already present.

The time slot extraction circuit uses the timings CK/SYNC and

the extraction synchronisms to load in first shift registers the time slots of the flows 2MSN.IN when the respective extraction synchronisms happen. Immediately after loading, the content of the shift registers is unloaded in parallel in second shift registers to  
5 whose clock inputs arrive the pluralities of signals LAPD.CK. The serial signals emerging from said registers are the pluralities of numerical flows LAPD.LK.IN. The insertion circuit for time slots belonging to the flows LAPD.LK.OUT in the numerical flows 2MSN.OUT operates in a perfectly dual manner.

10 With reference to FIG. 3, in which the same elements as in FIG. 2 are indicated by the same symbols, there is now illustrated in detail the second processing unit DSP.CIRCUITS of FIG. 2. In the figure, the symbol DSP16A indicates an AT&T microprocessor DSP 16A characterized in that it has a first 16-line bus 11 on which are  
15 multiplexed the addresses and data, both 16-bit, and two other busses INDR and COD on which the addresses and data are available separately. The microprocessor generates control signals CONTR for governing the read and write operations, performed through the bus 11, to external devices. For this purpose said bus is connected to  
20 latches IND.LTC and transceiver DAT.TRS to which arrive the control signals CONTR for demultiplexing of the addresses in an address bus 11.IND and of the data in a data bus 11'.D.

An oscillator OSC, also belonging to the DSP.CIRCUITS unit, sends to the microprocessor DSP16A a 40MHz clock signal to time its  
25 operation. To the busses INDR and COD is connected an EPROM indicated by the symbol EPROM in which is memorized the program (firmware) performed by the microprocessor DSP16A. The configuration of the address bits present on the bus 11.IND is decoded by a logic circuit to which arrive also the signals CONTR and which generates  
30 four enablement signals (chip select) CS0, CS1, CS2 and CS3 directed to a static RAM indicated by the symbol RAM, to a direction and control point register SC.REG and, through the bus 11.DAT, to the memory DUAL.PORT.0 of FIG. 2 and its semaphores respectively. The busses 11.IND and 11'.D and the signals CONTR of the microprocessor  
35 DSP16A arrive at the RAM, the register SC.REG, and a parity generation and verification circuit indicated by PR.AL.GEN.

Said circuit, at each write operation performed by DSP16A,

generates parity bits on as many lines associated with the bus 11'.D and, during each read operation, verifies the parity on the data read from the bus 11'.D. It is noted that the bus 11.DAT corresponds to the bus 11'.D with the addition of lines for the signals CONTR and  
5 for the enablement signals CS2 and CS3. In case of parity error there is generated the alarm signal ALARM-DSP sent to the unit 80C186.CIRCUITS of FIG. 2 and to the microprocessor DSP16A as an interrupt signal INT.

As regards the size of the memory indicated by RAM, it should  
10 be premised that said memory is used to store the information deriving from transmission measurements contained in messages for 100 different signaling channels which can be active simultaneously and each having available 1024 words for its own needs. Since the addressing capacity of the DSP16A is 64 kwords while the overall RAM  
15 space necessary for the job for which the microprocessor is assigned exceeds said capacity, the solution adopted was to use a memory having 128 kwords of 16-bit divided in two separately accessible 64 kword pages. Access is completed in two consecutive bus cycles, of which the first is used to write a control point PG in the register  
20 SC.REG for the choice of the memory page 0 or 1 to which it accedes during the second cycle. The DSP16A avoids performing the first access cycle, writing of the control point PG, if it is not necessary to change page. In each of the two RAM pages the area actually used to memorize the data which concern the channels is of only 56 kwords  
25 while the remaining area is unused.

The addressing space included in the 56 kwords used for the RAM and the 64 kwords actually addressable by the DSP16A is used by the latter to accede to the register SC.REG, to the DUAL.PORT.0 and to the related semaphores regardless of the value of the control point  
30 PG and in a single bus cycle.

Another 128 kbytes divided in two 64-kbyte pages are available for memorizing the parity bits associated with the bus 11'.D.

The microprocessor DSP16A writes in the register SC.REG three control points of which one is the above control point PG; the other  
35 two originate two respective signals FRZ-AL and RES-AL sent to the circuit PR.AL.GEN to verify correct operation thereof. The signal FRZ-AL forces generation of the signal ALARM-DSP while RES-AL zeroes

it. The active signal ALARM-DSP originates in the register SC.REG a sense point bit read when needed from DSP16A.

The AT&T microprocessor DSP 16A is specialized in the performance of arithmetic operations and therefore lends itself well to carrying out the functions which will be seen better below. As was said above, it communicates with the processing unit 80C186.CIRCUITS of FIG. 2 through the memory DUAL.PORT.0 to which it accedes by means of the busses 11.IND and 11.DAT. On a separate way the unit 80C186.CIRCUITS sends to the DSP16A the reset signal RESET-DSP when it serves.

There is now explained the operation of the telephone signaling processor represented by the block PPLD, first considering operation of the microprocessor 80C186 which processes the protocol LAPD and makes the microprocessor DSP16A able to perform the higher level processing. Subsequently operation of the latter is explained.

It is useful to recall that the purpose of the protocol LAPD, which operates on level 2 messages, is to convey information between level 3 entities through a user/network interface of the A-bis type or equivalent (ISDN). The structure with multiple hierarchical levels allows division of the signaling protocol functions in a succession of independent levels in which each level makes use of the communication services made available by the lower level and offers its own to the higher level. The level 2 messages comprise generally a numbering field, a head field and a tail field, an informative content, an address, and control fields. The level 2 messages, termed also 'frames', are optionally preceded and followed by filling frames free of informative content. The structure of the frames is defined by CCITT Recommendation Q 921.

The microprocessor 80C186 first analyses the various fields of the level 2 messages which reach it on the channels LAPD.LK.IN and obtains information on the basis of which it carries out the level 2 functions (described in GSM protocol 08.56) which concern management of the connection between BTS and BSC to ensure regular flowing of the planned flow of level 3 messages between the BTS and the telephone processor TDPC or directly between MS and TDPC. Said level 3 messages are mainly those of the protocols denominated RR', RR\* and BTSM (BTS Management) described in GSM Recommendation 08.58 in which

- 28 -

BTSM allows dialog between BSC and BTS; RR' and RR\* constitute the radio protocol RR which manages the functions of Power Control, Frequency Hopping, Configuration of the channels on the radio frame, Cipherring, and Handover; specifically, RR' allows dialog between MS and BTS; and RR\* allows dialog between MS and BSC, passing transparently through BTS.

In the flow chart of FIG. 4 detailed indications on the different types of message are not given. FIGS. 5, 6a and 6b examine in greater detail the subset of messages belonging to the unit DSP16A. In addition, said chart does not show any exchange of messages between PPLD and the administrative processor MPCC. This does not mean that an exchange does not occur. In reality, between MPCC and PPLD information is exchanged mainly on the hardware and software configuration of PPLD, the operations to be undertaken for maintenance of the board, and the values of some E&M parameters used in the application programs. Said information does not fall within the type of messages as they are understood from the signaling viewpoint and therefore the figure does not show any message concerning it.

The flow chart of FIG. 4, in which the elements common to FIGS. 1, 2 and 3 are indicated by the same symbols, comprises the following phases:

- a start phase 0 in which the microprocessor 80C186, referred to hereinafter as CPU, performs a microprogram to prepare appropriately the status of the various registers and devices used, after which it activates the protocol LAPD by sending on the flows LAPD.LK.OUT frames containing special activation messages addressed to each TRX of every BTS respectively and then waits to receive on the flows LAPD.LK.IN corresponding frames backward comprising the correct answer messages from each TRX. When this has occurred the protocols LAPD are activated for all the TRX of the BTS leading to the BSC. Said protocols remain activated for an indefinite time, at least until the network is reconfigured and in this case the protocols are deactivated by an equivalent procedure. After the activation phase the program enters phase 1 in which the CPU prepares memory areas, termed hereinafter buffers, in which to store the message queues to be sent to the BTS, to the telephone

- 29 -

processor TDPC, to the administrative processor MPCC and to the microprocessor DSP16A, termed hereinafter DSP, respectively. Buffers of equivalent size are reserved for storage of the queues of message from BTS, DSP, TDPC and MPCC. Said buffers are

5 physically located in the working memory of the CPU and in DUAL.PORT.0 and DUAL.PORT.1. The messages are inserted in the respective queues in the order in time in which they were acquired or generated and are taken in decreasing priority order which assigns the highest priority to the oldest message in the queue.

10 With every buffer is associated a semaphore whose purpose is to discipline write and read access, and an indicator of the buffer fill status.

- the CPU then enters phase 2 in which it checks if it has received a reception interrupt from one of the serial communication devices

15 HSCX corresponding to the sending of a valid LAPD message by a TRX of a BTS and, if has this occurred, phase 3 is performed but otherwise there is a jump to phase 10 which will be discussed below;

- in phase 3 are performed the level 2 operations which concern the

20 message reception process and specifically the level 2 frames are memorized by checking the head and tail fields and the CRC (Cyclic Redundancy Control) field which indicates the integrity of the message received. There is also checked the order of arrival of the various frames and, if it does not correspond to a correct

25 sequence, the latter is restored. In case of lacking messages there is requested a retransmission. In case of corrupt bits the CPU attempts to correct the errors. After completion of this phase, if all has gone well, the program goes into phase 4 in which the message is memorized in the buffer of the messages coming from

30 the BTS;

- the program then enters phase 5 in which is analyzed the address field of the message to establish to whom said message is addressed. For this purpose, in the following phase 6 there is performed a test to establish whether the addressee of the message

35 from the BTS is the telephone processor TDPC or DSP. If the addressee is TDPC the message is memorized in the buffer of messages to be sent to TDPC, but if the addressee is DSP the

- 30 -

- message is memorized in the buffer of messages to be sent to DSP; -  
in the following phase 7 the CPU performs a process of transfer to  
TDPC of the above message. The process starts with cyclic  
interrogation by the CPU of a semaphore of the DUAL.PORT.1 until it  
5 is free and in this case the CPU engages it and writes the message  
in the DUAL.PORT.1, after which it releases the semaphore. At this  
point with an equivalent procedure the processor TDPC can read the  
message transferred to it. After performing phase 7 the program  
jumps to a point A preceding phase 2 in which the CPU waits for a  
10 reception interrupt of a new LAPD message.
- The program reaches phase 8 if in the preceding phase 6 the  
addressee of the message from the BTS is DSP. In this case the CPU  
takes the message from the buffer of messages to be sent to DSP and  
completes a reformatting thereof consisting of selecting the  
15 informative content and some control fields, taking a message for  
DSP;
  - in the following phase 9 the CPU performs a process of message  
transfer to DSP. The process begins with the cyclic interrogation  
by CPU of the semaphore which regulates access to the buffer of  
20 DUAL.PORT.0 in which are memorized the messages to be sent to DSP.  
Hereinafter, when discussing FIGS. 9 and 10, said semaphore will be  
indicated by SEM\_TX. When the semaphore is free the CPU engages it  
to prevent any read access by DSP and writes the message in the  
buffer, after which it releases the semaphore and the program jumps  
25 to point A.
  - The program reaches phase 10 if in phase 2 there occurred no  
reception interrupts of LAPD messages. All the phases described  
subsequently are for the activity normally carried out by the CPU  
during the time between the interrupts received in phase 2. This  
30 activity consists principally of acquisition of messages by TDPC  
and DSP and in the transfer thereof to the respective addressees.  
In phase 10 the CPU interrogates cyclically a semaphore of the  
DUAL.PORT.1 until it is free and in this case the CPU engages it  
and reads in DUAL.PORT.1 the logic value of the fill status  
35 indicator of the buffer of the messages coming from TDPC. This  
last operation corresponds to the test of the next phase 11  
performed to verify whether in said buffer there is no message;



- 31 -

- 5     - if the condition of phase 11 is not verified it means that one or more messages are present in the buffer. In this case the CPU keeps the semaphore engaged and performs phase 12 in which it reads the first message of the queue present in DUAL.PORT.1 after which it releases the semaphore;
- 10    - in the following phase 13 the CPU performs a test on the address field of the message just read to establish if it is addressed to BTS or to DSP. If the addressee is BTS the message is memorized in the buffer of messages to be sent to BTS and otherwise is memorized in the buffer of the messages to be sent to DSP. After which the CPU performs phase 14, at the end of which the program jumps to point A.
- 15    - In phase 14 the CPU performs a process of sending the message to the TRX addressee. The process starts with writing of a control point in a serial communication device register HSCX which generates the flow LAPD.LK.OUT to said TRX. Upon reception of the control point there follows the sending by HSCX of a transmission interrupt to the CPU, which transfers the message from the buffer in which it is found to a transmission buffer in HSCX and the process is thus completed.
- 20    - The program reaches phase 15 if in the preceding phase 13 the addressee of the message coming from TDPC is DSP. In this case there are performed phases 15 and 16 which are the same as phases 8 and 9, after which the program jumps to point A.
- 25    - The program reaches phase 17 if in the preceding phase 11 the queue of messages sent from TDPC to CPU is empty. In phases 17 and 18 the CPU verifies the presence of messages in the queue of messages from DSP; as may be imagined, phases 17 and 18 are like phases 10 and 11 but apply to DSP and DUAL.PORT.0. If from the test of the phase 18 the queue of messages from DSP is empty, the program jumps to point A but otherwise phase 19 is performed;
- 30    - in phase 19 the CPU performs a process of message reception from DSP. The process begins with cyclic interrogation by the CPU of the semaphore which regulates access to the buffer of DUAL.PORT.0 reserved for messages received from DSP. In the comments on FIGS. 9 and 10 below said semaphore is indicated by SEM\_RX. When the semaphore is free the CPU engages it to prevent any write accesses
- 35

- 32 -

- by DSP and reads the first message of the list of messages present in the buffer, after which it releases the semaphore;
- in the following phase 20 the CPU performs a test on the address field of the message just read to establish if it is addressed to BTS or to TDPC. If the addressee is BTS the message is memorized in the buffer of messages to be sent to BTS but otherwise it is memorized in the buffer of the messages to be sent to TDPC. After which the CPU performs phase 21 which is the same as phase 14. At the end of phase 21 the program jumps to point A.
  - The program reaches phase 22 if in the preceding phase 20 the addressee of the message from DSP is TDPC. In this case the CPU performs phase 22 which is the same as phase 7 and then the program jumps to point A.

FIG. 5 shows some messages indicated in FIG. 4 by the generic term 'message' and specifically those regarding DSP. The figure shows two groups of messages indicated by the names assigned them by GSM Recommendation 01.04. A first group comprises the following messages: MEASUREMENT\_RESULT, CHANGE\_BS\_POWER and CHANGE\_MS\_POWER of which the first comes from BTS while the other two are directed to BTS. A second group comprises the following messages: HO\_CANDIDATE\_ENQUIRE\_INVOKE, HO\_CANDIDATE\_ENQUIRE\_COMPLETE, CONDITION\_FOR\_INTRA\_CELL\_HO, CONDITION\_FOR\_INTER\_CELL\_HO, RESET and MS\_RF\_POWER\_CAPABILITY, of which the first, third and sixth messages come from TDPC while the second, fourth and fifth are directed to TDPC. With further reference to FIG. 4 the message MEASUREMENT\_RESULT is the one transferred in phase 9. The messages CHANGE\_BS\_POWER and CHANGE\_MS\_POWER are those transferred in phase 21. The messages HO\_CANDIDATE\_ENQUIRE\_INVOKE, RESET and MS\_RF\_POWER\_CAPABILITY are those transferred in phase 16. And lastly the messages HO\_CANDIDATE\_ENQUIRE\_COMPLETE, CONDITION\_FOR\_INTRA\_CELL\_HO and CONDITION\_FOR\_INTER\_CELL\_HO are those transferred in phase 22. It will be seen shortly that, in reality, some of the messages directed to BTS and TDPC continue to MS and MSC respectively, just as some messages from BTS and TDPC are originated by MS and MSC.

The messages of FIG. 5 are explained below in the order in which they appear in the figures: MEASUREMENT\_RESULT comprises the

- 33 -

values of the transmission measurements performed by MS and BTS in the course of the calls, as per GSM Recommendation 05.08 including Appendix A. The content of this message is the subject of a large part of the processing performed by the DSP and a more detailed representation of this is therefore given in FIGS. 6a and 6b.

CHANGE\_BS\_POWER is a command given to a TRX of a BTS to change in the indicated manner the transmission power for a certain channel indicated as per GSM Recommendations 08.58 and 05.08.

CHANGE\_MS\_POWER is a command given to an MS to change in the indicated manner the power of its transmitter as per GSM Recommendations 04.08 and 05.08.

HO\_CANDIDATE\_ENQUIRE\_INVOKE comprises indication of a list of cells in which for each cell of the list and for a subset of mobiles associated with the cell the DSP must start the homonymous Handover procedure to transfer said mobiles to other cells, as set forth in GSM Recommendations 08.08 & 3.1.8. This message is sent by MSC which requires a Handover for traffic reasons.

HO\_CANDIDATE\_ENQUIRE\_COMPLETE is a message sent to MSC to close the procedure started by the preceding message.

RESET releases the resources made available to a channel which is closed due to end of communication.

CONDITION\_FOR\_INTRA\_CELL\_HO comprises a command which TDPC must send to an MS and to the BTS of the serving cell so that an Intracell Handover will be carried out as per GSM Recommendations 05.08 and 08.08 & 3.1.6.

CONDITION\_FOR\_INTER\_CELL\_HO comprises a command which TDPC or optionally MSC must send respectively to an MS, to the BTS of the presently serving cell, and to a BTS of an adjacent cell which will become the new serving cell so that an Intercell Handover will be carried out as per GSM Recommendations 05.08 and 08.08 & 3.1.7. The message contains a list of preferred cells.

MS-RF-POWER-CAPABILITY comprises an indication of the mobile power class, i.e. of the upper power limit which can be reached by the MS transmitter.

With reference to FIGS. 6a and 6b a table sets forth the main fields contained in the message MEASUREMENT\_RESULT called by the names assigned to them by GSM Recommendation 01.04. Said message

respects the cadence of the multiframe SACCH which has a period of approximately 480 ms, which corresponds to the time of 104 base frames. When the function 'Discontinuous Transmission' is active, some fields of the message comprise a suffix \_SUB, because the measurements are averaged on a subset of 12 frames out of 104 and in the opposite case comprise a suffix \_FULL. Said fields also comprise a suffix \_DL, which stands for downlink, if the measurements are completed by MS; but they comprise a suffix \_UP, which stands for uplink if the measurements are completed by BTS.

10       The meaning of the various fields is as follows:  
MESSAGE\_TYPE: level 3 control field which indicates the type of message among those of FIG. 5 to which the fields relate; in the case in question the message is obviously that of MEASUREMENT\_RESULT;  
D|TEI|CHANNEL\_NBR: level 2 fields in which field D identifies the number of the flow LAPD.LK.IN which carries the message to DSP; the field TEI identifies the TRX, within BTS, from which comes the signaling channel transferred onto the flow D, which is equivalent to defining the transmission and reception carrier pair; the subfield CHANNEL\_NBR identifies the time slot number assigned to the mobile  
15       for use with time division of said carrier pair, i.e. it identifies the voice channel TCH and the channel SACCH involved with the message.

The following fields are all level 3 and constitute the information content of the message:

25       DTX\_DL and DTX\_UL: indicate whether the carrier of a channel TCH has been actually transmitted in the previous frame. As concerns the channels SDCH, in particular SACCH, the transmission procedure DTX is not used;

30       RXLEV\_FULL\_DL, RXLEV\_SUB\_DL, RXLEV\_FULL\_UP, RXLEV\_SUB\_UP: indicate the level of the channel TCH in use, respecting the FULL/SUB and DL/UP procedures;

35       RXQUAL\_FULL\_DL, RXQUAL\_SUB\_DL, RXQUAL\_FULL\_UP, RXQUAL\_SUB\_UP: indicate the quality of the channel in use expressed by the value of the related BER (bit error rate), respecting the FULL/SUB and DL/UP procedures;

TIMING\_ADVANCE: indicates the value of the homonymous parameter for the channel in use;

- 35 -

No\_CELL: indicates the total number of adjacent cells present in the MEASUREMENT\_RESULT message; it is a number which can vary from 0 to 6.

5 RXLEV\_NCELL\_1: indicates the level of the carrier BCCH of an adjacent cell located in the first position in a list of 6 cells whose carriers BCCH are sensed by the mobile with a stronger level. In reality the mobile can measure the level of 32 adjacent cells, however each MEASUREMENT\_RESULT message, because of length problems, only comprises 6 of them which can thus vary from one message to the  
10 next.

BSIC\_BCCH\_1: contains the cell code number and the frequency value of the carrier BCCH of the first cell of said list compiled by the mobile;

15 RXLEV\_NCELL\_N: indicates the level of the carrier BCCH of the Nth cell of said list;

BSIC\_BCCH\_N: contains the cell code number and the frequency value of the carrier BCCH of the nth cell of said list.

All of the above fields are read by DSP in DUAL.PORT.0 and written dynamically in the external RAM of the DSP using for this purpose  
20 pointers, memorized in said external RAM, which refer to respective addressing tables contained in the internal RAM of the DSP.

With reference to FIG. 7 there can be seen the image of a part of the internal memory of the DSP just after termination of the initialization phase. As can be seen, it comprises a sequential list  
25 of 100 addressing tables three words long each and concatenated by means of pointers FRETAB00, ... FRETAB99 which indicate the address of the first word of the respective table to which they point. Each table is associated with a respective channel whose transmission measurement values must be processed; it contains an indication on  
30 the position of the external RAM of the DSP where there is temporarily allocated an area of 1024 consecutive words reserved for the fields of the message being processed. The meaning of the three consecutive words of which is made up each table is the following: in the first word is memorized the starting address of the following  
35 table concatenated in the list and it is therefore one of said pointers; the second word consists of a single significant bit whose value zero or one means that the memory area reserved for the channel

is located on page zero or one of the external RAM of the DSP; the third word is the starting address of the respective external memory area temporarily assigned to the channel. The hexadecimal value of said address is between 1000 and D400 in both pages of the external RAM. At the head of the table list is allocated a pointer FRETABPTR which indicates the address of the first free table in the list.

In FIG. 7 the pointer FRETABPTR coincides with the starting address FRETAB00 of the first table of the list because initially the tables are obviously all free, and the pointer contained in each table refers back to the address table immediately increasing. The pointer belonging to the last table, memorized at the address FRETAB99, possesses a hexadecimal value FFFF, which does not correspond to another concatenated table but will later be interpreted as the fact that in the external RAM there are no more areas available for the channels.

With reference to FIG. 8 in which the same elements of FIGS. 6a, 6b and 7 are indicated by the same symbols there is visible an image of page 0 of the external RAM to which accedes the DSP. In the memory page the areas assigned to the channels have been allocated in conformity with the contents of the address tables of FIG. 7. The initial part of the memory starting from the address 0 up to the address 2047 is an area PTR of 2048 words reserved for memorization of the pointers of the 100 address tables of FIG. 7 with a mechanism which will be clarified when FIG. 14 is discussed. Initially the area PTR is empty. Then, by the acquisition of the messages to be processed by the DSP, it is filled up to a maximum of 100 words distributed randomly in the available area. The addresses of the words of the PTR area are obtained by decodification of the 11 bits of the fields D, TEI and CHAN\_NBR of the messages which reach the DSP. The bit 15 of a generic word, indicated by a, is written with value 1 every time an external RAM area is assigned to the corresponding channel and restored to value 0 when the area in question is freed. The remaining bits of the word indicate any pointer FRETAB00, ... FRETAB99, generically denominated FRETABXY.

The fields D, TEI and CHAN\_NBR allow unequivocal identification, for purposes of processing the transmission measurements, of any channel among all those theoretically possible

- 37 -

within a cluster of cells governed by a BSC. As was mentioned above, for the GSM system the maximum number is 1984 half-rate channels. But in practice the maximum number of channels actually usable is smaller because a larger number of full-rate channels is planned and because not all transceivers are initially fitted out within the BTS. Even thus, the maximum number of usable channels exceeds that of the respective 100 memory areas planned for them. But the fact does not cause inconveniences since the capacity of the DSP to process 100 channels simultaneously should be sufficient to ensure service even in peak traffic periods. Indeed, the value 100 was obtained by utilizing calculation methods typical of telephone traffic theory starting from a situation reflecting that of a cluster of cells with known traffic characteristics. If with the passage of time there should occur a remarkable increase of mobile radio telephone traffic within the preselected cluster it is sufficient to fit out additional PPLD boards (FIG. 1) in the controller BSC.

In FIG. 8 there can also be seen the actual arrangement of the fields of FIGS. 6a and 6b in a memory area assigned to a first channel starting from the address 1000H supplied by the first table (FRETAB00) of FIG. 7. By analogy, the same arrangement applies even for all the remaining 49 areas of page 0 and for the 50 areas of page 1.

Inside the area assigned to the 1st channel there can be seen two subareas indicated by CELL.SER and CELL.AD, for the serving cell and the adjacent cells respectively. The subarea CELL.SER comprises five groups of words indicated by G1, G2, G3, G4 and G5 respectively; the groups follow each other in the order given. Immediately after the group G5 is allocated a single word MS\_RF\_CAP also belonging to the area CELL.SER, coming from the message MS\_RF\_POWER\_CAPABILITY. The groups from G1 to G5 comprise respective sequences of 32 words of memory reserved for the memorization of as many sequential values of some fields of the MEASUREMENT\_RESULT message which will be listed shortly. In this manner there are available in memory for each of the fields to be processed the values for the last 16 seconds (32 x 480ms) of operation.

The above said sequences are treated by the software in such a manner as to simulate, as concerns the processing phases, as many

shift registers which expel the oldest value upon each acquisition of a new value. To comply with the operating procedures mentioned above, the groups from G1 to G5 comprise 33rd and 34th words used as modulus 32 counters to address the words within the respective sequences as will be clarified below.

The meaning of the various groups is as follows:

- group G1 memorizes the value of the field RXLEV\_FULL\_UP or alternatively of the field RXLEV\_SUB\_UP, the 33rd word is indicated by INBF\_LU and the 34th word by DEBF\_LU;
- 10 - group G2 memorizes the values of the field RXQUAL\_FULL\_UP, or alternatively of the field RXQUAL\_SUB\_UP, the 33rd word is indicated by INBF\_QU and the 34th word by DEBF\_QU;
- group G3 memorizes the values of the field TIMING\_ADVANCE, the 33rd word is indicated by INBF\_TA and the 34th word by DEBF\_TA;
- 15 - group G4 memorizes the values of the field RXLEV\_FULL\_DL, or alternatively of the field RXLEV\_SUB\_DL, the 33rd word is indicated by INBF\_LD and the 34th word by DEBF\_LD;
- group G5 memorizes the values of the field RXQUAL\_FULL\_DL, or alternatively of the field RXQUAL\_SUB\_DL, the 33rd word is indicated by INBF\_QD and the 34th word by DEBF\_QD.
- 20

Subarea CELL.AD comprises a space for sixteen subtables for as many cells adjacent to the serving cell. Each subtable is made up of 36 consecutive words of which the first contains the field BSIC\_BCCH(*n*), by  $n \ 1 \leq n \leq 16$ ; the second word is a mean value AV\_RXLEV\_NCELL(*n*) calculated as will be seen in a short while. The words from 3 to 34 correspond to 32 values of the field RXLEV\_NCELL(*n*); and lastly the 35th and 36th words indicated by INBF\_LD(*n*) and DEBF\_LD(*n*) respectively are used as modulus 32 counters like those of groups G1 to G5. As regards the relationship between the index *N* of the fields BSIC\_BCCH(*N*), RXLEV\_NCELL(*N*) read in the MEASUREMENT\_RESULT message and the index *n* of said fields when they are written in the corresponding *n*th subtable, there will be given adequate explanations with the discussion of FIGS. 11 and 12.

35 The 15th bits of the words BSIC\_BCCH(*n*) are indicated by *b*, written with value 1 when the corresponding subtables are occupied, and written with value 0 when said subtables are free.

The information contained in the memory words of FIG. 8 are



- 39 -

those coming from MEASUREMENT\_RESULT messages but they are also used inside the INVOKE procedure for the pair of messages

HO\_CANDIDATE\_ENQUIRE\_INVOKE, HO\_CANDIDATE\_ENQUIRE\_COMPLETE.

5 With reference to the flow chart of FIGS. 9 and 10 there is now discussed the main program governing the operation of the DSP. The program comprises the following phases:

- an initial phase F0 in which the DSP writes in its internal RAM the table configuration of FIG. 7 and zeroes the external RAM. The details of the operations completed in this phase will be given with the discussion of FIG. 13. In this phase there are also written in the internal RAM all the E&M parameters necessary for the subsequent processing.
- The program then goes into phase F1 in which the DSP completes a cyclic interrogation of the semaphore SEM\_TX of the DUAL.PORT.0 until it finds it free. During occupation of the semaphore SEM\_TX the CPU is writing a message in the buffer of the messages to be sent to DSP allocated in the DUAL.PRT.0;
- as soon as SEM\_TX is free the program enters phase F2 in which the DSP engages the semaphore SEM\_TX and reads from the above said buffer the field MESSAGE\_TYPE of the highest priority message;
- in phase F3 is performed a test on MESSAGE\_TYPE to verify whether the related message is a MEASUREMENT\_RESULT message; if it is, the program jumps to phase F19 for treatment thereof, otherwise it goes into phase F4 in which is repeated the test on the field MESSAGE\_TYPE to verify whether the message in question is the MS\_RF\_POWER\_CAPABILITY type;
- if it is, the program goes in to phase F5 in which is called and performed a subprogram INDINAM which finds dynamically the memory area associated with the channel.
- In the following phase F6 is updated the value of the field MS\_RF\_CAP which indicates the power class of the mobile, i.e. the maximum power deliverable by the transmitter. After which, in phase F7, is released the semaphore SEM\_TX to allow the CPU to write other messages in the buffer of messages to be sent to DSP.
- 35 Next the program jumps to a point B between phases F0 and F1 for repetition of the new message acquisition cycle;
- if in phase F4 the answer is 'no' the program jumps to phase F8 in

- 40 -

which is repeated the MESSAGE\_TYPE test to verify whether the message in question is the RESET type;

- if it is, the program goes into phase F9 in which is called and performed a subprogram RILCAN for freeing of the external RAM memory area associated with the channel. In the following phase F10 is released the semaphore SEM\_TX and the program jumps to point B;
- if in phase F8 the answer is 'no' the program jumps to phase F11 in which is repeated the MESSAGE\_TYPE test to verify whether the message in question is of the HO\_CANDIDATE\_ENQUIRE\_INVOKE type;
- if the answer is 'no' the program goes into phase F12 in which is released the SEM\_TX semaphore, after which there is a jump to point B;
- if in phase F11 the answer is 'yes' the program jumps to phase F13 in which is released in this case too the semaphore SEM\_TX;
- in the following phase F14 is performed the INVOKE procedure which is very similar to the HANDOVER procedure activated by the MEASUREMENT\_RESULT message on condition of having at least one cell included in the list of preferred cells given at the end of the HANDOVER procedure coinciding with a cell of the list indicated in the HO\_CANDIDATE\_ENQUIRE\_INVOKE message. Since the HANDOVER procedure will be discussed in detail below, for the sake of brevity further details on the INVOKE procedure are not supplied.
- In the following phase F15 the DSP completes an interrogation cycle of the semaphore SEM\_RX of the DUAL.PORT.0 until it finds it free. During occupation of the semaphore SEM\_RX the CPU is reading a message in the buffer of the messages received from DSP allocated in the DUAL.PORT.0;
- as soon as SEM\_RX is free the program enters phase F16 in which the DSP engages the semaphore SEM\_RX and, in phase F17, writes in said buffer the HO\_CANDIDATE\_ENQUIRE\_COMPLETE message.
- In the following phase F18 is released the semaphore SEM\_RX after which there is a jump to point B.

Now having exhausted the considerations on the main messages which reach the DSP, the discussion left in suspense in phase F3 when the MESSAGE\_TYPE field indicated a MEASUREMENT\_RESULT message is resumed. In this case the program called for a jump to phase F19.

- 41 -

- In phase F19 is performed the subprogram INDINAM, similarly to what took place in phase F15;
- in the following phase F20 is called and performed a subprogram LETMESS which updates the sequences of 32 values of FIG. 8 reserved for the present channel. The new field values are written in predetermined positions within the external RAM area reserved for the channel whose starting address is given by the subprogram INDINAM as will be seen better from the discussion of FIGS. 11, 12 and 14. After which, in phase F21, is released the semaphore SEM\_TX and the program goes into phase F22 in which the processing executed on the memorized sequences in starting.
- In phase F22 is interrogated a field E&M denominated WAVT\_FL to establish which type of mean was preselected as a first step of the subsequent processing. As regards only the fields which are influenced by the Discontinuous Transmission, i.e. RXLEV and RXQUAL, two different types of weighted mean are possible: 'classical' weighted mean and 'accordion type' weighted mean; for all the other fields of FIG. 8 is applied a normal arithmetical mean. The means are calculated with a cadence which respects that of reading of the messages from the DUAL.PORT.0. Calculation of the means is done allowing for respective pairs of E&M parameters denominated Hreqave and Hreqt. The first parameter indicates the number of consecutive samples which enter into the mean; the second indicates the number of subsets, of Hreqave samples each, on which a mean is made. Logically there must be respected the condition  $Hreqave \times Hreqt \leq 32$ . The purpose is to generate a representation for points of the behaviour in time of the averaged magnitude, an operation termed 'trend analysis'.
- If in phase F22 the choice falls on the classical weighted mean, the program goes into phase F23 in which for each subset Hreqt, in a generic sequence, the following expression is calculated.

$$\frac{p_1 \sum_{i=1}^m C_i + p_2 \sum_{j=m+1}^n C_j}{mp_1 + (n - m)p_2}; \quad (1)$$

in which:  $C_i$  is a generic sample SUB;  $p_1 = 1$  is the weight of the generic sample SUB;  $C_j$  is a generic sample FULL;  $p_2$  is the weight

- 42 -

- of the generic sample FULL;  $n = H_{reqave}$ ;  $m$  is the number of the SUB samples on the  $n$  taken into consideration in the formula (1). As the samples FULL are more reliable than the SUB samples, they enter into the mean with greater weight, thus  $p_2 > p_1$ . The expression
- 5 (1) is calculated for each new message for all the subsets  $H_{reqt}$ , which must then present to the calculation values updated with the same cadence as (1). In effect this takes place, in view of what was said about shifting of the words inside the respective sequences. Calculation of (1) is suspended for a time  $H_{reqave} \times$
- 10 480ms upon reception of the first MEASUREMENT\_RESULT message so that the mean can actually be calculated on  $H_{reqave}$  values. The mean for the subsets  $H_{reqt}$  will gradually go to steady condition within 16 seconds.
- In phase F24 the means calculated in the preceding phase are
- 15 compared with a first group of thresholds for the Power Control and then with a second group of thresholds for the Handover, and in both cases the threshold values are available as E&M parameters. The comparison is the multiple type and makes use for the purpose of numbers pairs  $P_x$ ,  $N_x$  associated with the thresholds, and these
- 20 also available as E&M parameters. A generic threshold  $X$  is considered crossed over when on  $N_x$  comparisons at least  $P_x$  are positive, since the prevailing condition is  $N_x > P_x$ . As regards the Power Control, for each averaged magnitude there are two thresholds, one lower and one upper. The compared means are
- 25 those for the magnitudes  $RXLEV_{(FULL/SUB)}_{UL}$ ,  $RXQUAL_{(FULL/SUB)}_{UL}$ ,  $RXLEV_{(FULL/SUB)}_{DL}$  and  $RXQUAL_{(FULL/SUB)}_{DL}$ . The magnitudes with suffix  $_{DL}$  supply indications for checking the power transmitted by BTS; those with suffix  $_{UL}$  supply indications for checking the power transmitted by an MS.
- 30 As regards the Handover, for every magnitude averaged there is a single comparison threshold. The means compared are all those for the magnitudes taken into consideration for the Power Control plus those for the TIMING\_ADVANCE appropriately converted to a distance value DIST according to a known formula.
- 35 - Returning to the test of phase F22, if in this phase the choice falls on the weighted mean of the 'accordion type', the program goes into phase F25 in which is calculated an expression which

- 43 -

differs from (1) in that the sum of the weights is constant and equal to Hreqave, while the number of samples taken into consideration for the mean varies consequently. This type of mean is preferable in some typical situations since it is faster to calculate. The description of the following phase F26 is like that of phase F24.

- Both phases F24 and F26 converge in phase F27 in which are calculated the 'unweighted' arithmetical means on each of the  $n$  sequences  $RXLEV\_NCELL\_n$  relative to the adjacent cells, using in the aforesaid manner the parameters Hreqave and Hreqt. For every sequence the mean corresponding to that of the most recent subset (Hreqave) is indicated in FIG. 8 by  $AV\_RXLEV\_NCELL\_n$ . During calculation there may occur the situation in which from a certain moment forward the messages no longer contain the fields of a certain sequence  $RXLEV\_NCELL\_x$ , which means that the related adjacent cell is no longer perceived by the mobile as one of the 6 strongest. In this case calculation of the mean continues taking on null value for the missing fields until the mean cancels itself and the respective sequence becomes available again for another adjacent cell after zeroing of the bit  $b$  of the word  $BSIC\_BCCH\_n$ .
- The program continues with phase F28 in which the  $AV\_RXLEV\_NCELL\_n$  means are used for calculating as many merit parameters termed 'Power Budget', each for one of its own adjacent cells, which indicate the quality of the radio connection between the mobile and the BTS of the adjacent cell. In GSM Recommendation 05.08, version 3.7.0, Appendix A, paragraph 3.1, sub-section f, is given a mathematical function  $PBGT(n, x1, x2, x3)$  which allows calculation of the Power Budget for a generic adjacent cell ( $n$ ). The variables  $x1, x2, x3$  consist of E&M constant magnitudes and of variable magnitudes of  $RX\_LEV\_FULL\_DL$  mean type of the serving cell, and  $AV\_RXLEV\_NCELL\_n$  of the adjacent cell  $n$  to which the calculation refers. Specifically, the variable  $x1$  represents the difference in dB between the maximum transmission power in the serving cell and in the  $n$ th adjacent cell. The variable  $x2$  represents the difference between the path losses in the two above cells. The variable  $x3$  represents the difference between the

maximum powers usable by a mobile in the two cells.

The Power Budgets appraisable for each new message acquired are 6 which, in view of the above, do not necessarily relate to the same adjacent cells, as they can vary from one message to the next.

5 Herefrom arises the need to consider a larger number of adjacent cells, considered for convenience equal to 16. Still in phase F28, the Power Budgets PBGT(n) are compared with respective thresholds given as E&M parameters, taking values termed HO\_MARGIN(n), which will be used for the Handover decisions.

10 - In the following phase F29 is compiled a list comprising a maximum of 16 preferred cells with which the mobile could make a Handover. GSM Recommendation 05.08, Appendix A, paragraph 4, indicates an inequality of the type  $AV\_RXLEV\_NCELL(n) > K$ , as a preliminary condition for admitting an adjacent cell  $n$  to the list; K  
15 represents the sum of constant magnitudes given as E&M parameters. In compiling the list allowance is also made for the outcomes of the comparisons made in phases F24, or F26, and F28. Another criterion is verification of the coincidence between the 16 cells examined and those assigned by E&M as preferable. The cells appear  
20 in all the lists respecting in decreasing order of the values of HO\_MARGIN(n).

- In the following phase F30 are examined the results of the comparisons of phase F24, or F26, to decide on the Power Control. The conditions examined are the following:

25 1) the means remain inside the respective thresholds; in this case no action is taken and the program goes into phase F35 where there will be examined improbable Handover conditions;

30 2) the mean for  $RXLEV\_FULL/SUB\_UL$  is less than the respective lower threshold, or the mean for  $RXQUAL\_FULL/SUB\_UL$  exceeds the respective upper threshold;

in this case there is prepared a CHANGE\_BS\_POWER message to increase the power transmitted by BTS with a step defined by a special E&M parameter;

35 3) the mean for  $RXLEV\_FULL/SUB\_UL$  is greater than the respective upper threshold, or the mean for  $RXQUAL\_FULL/SUB\_UL$  is less than the respective lower threshold; in this case there is prepared a CHANGE\_BS\_POWER message to decrease the power transmitted by BTS

- 45 -

with a step defined by a special E&M parameter;

4) the mean for RXLEV\_(FULL/SUB)\_DL is less than the respective lower threshold, or the mean for RXQUAL\_DL exceeds the respective upper threshold; in this case there is prepared a CHANGE\_MS\_POWER message to increase the power transmitted by the mobile with a step defined by a special E&M parameter;

5) the mean for RXLEV\_(FULL/SUB)\_DL is greater than the respective upper threshold, or the mean for RXQUAL\_DL is less than the respective lower threshold; in this case there is prepared a CHANGE\_MS\_POWER message to decrease the power transmitted by the mobile with a step defined by a special E&M parameter. Any other conditions, which give rise to decision conflicts, are treated with priority for the decisions which derive only from the RXLEV\_(FULL/SUB)\_UL or RXLEV\_(FULL/SUB)\_DL magnitudes.

If the power increases or decreases have piloted the transmitters at the maximum power deliverable, or alternatively at the minimum allowed, it means that all the possibilities of the Power Control are exhausted. In this case, if any of the conditions from 2) to 5) persist, the program jumps to phase F35 but otherwise continues with phase 31.

- In phase F35 are examined the results of the comparisons of phases F24 or F26, and F28 to decide on the Handover. The conditions examined are the following:

1) the mean for RXLEV\_(FULL/SUB)\_UL or RXLEV\_(FULL/SUB)\_DL is less than the E&M threshold indicating the minimum allowed level;

2) the mean for RXQUAL\_(FULL/SUB)\_UL or RXQUAL\_(FULL/SUB)\_DL is greater than the E&M threshold indicating the maximum allowed BER level;

3) the mean for the magnitude DIST is greater than the E&M threshold indicating the maximum allowed distance;

4) the thresholds for RXLEV\_(FULL/SUB)\_UL (or RXLEV\_(FULL/SUB)\_DL) and RXQUAL\_(FULL/SUB)\_UL (or RXQUAL\_(FULL/SUB)\_DL) are simultaneously exceeded, i.e. the mobile or the BTS work with high power level and poor quality;

5) for Nx consecutive times the following inequalities are simultaneously true or simultaneously false:  $PBGT(n) > 0$ ;  $PBGT(n) > HO\_MARGIN(n)$ .

- 46 -

- Condition 4 gives rise to the preparation of a  
CONDITION\_FOR\_INTRA\_CELL\_HO message. Conditions 1, 2, 3 and 5  
give rise instead to the preparation of a  
CONDITION\_FOR\_INTER\_CELL\_HO message; of these only condition  
5 causes a Handover for 'BETTER CELL' and has lower priority.  
If none of the conditions from 1 to 5 occurs the program jumps  
directly to point B but otherwise continues with interrogation  
phases F36 and F37 and engagement of the semaphore SEM\_RX, like  
phases F15 and F16 already described.
- 10 - In the following phase F38 is written in DUAL.PORT.0 a Handover  
message which, on the basis of the conditions occurring in phase  
F35, can be either the CONDITION\_FOR\_INTER\_CELL\_HO message,  
comprising also the list of preferred cells compiled in phase F29,  
or that of CONDITION\_FOR\_INTRA\_CELL\_HO. After which in phase F39  
15 the semaphore SEM\_RX is released and the program jumps to point B.
- Taking up again the test performed in phase F30, if there are  
verified any of the Power Control conditions, the program performs  
phases F31 and F32 in which it interrogates the semaphore SEM\_RX  
and engages it, similarly to what was seen for phase F15 and F16.
- 20 - In the following phase F33 there is written in DUAL.PORT.0 a Power  
Control message which, on the basis of the conditions verified in  
phase F30, can be either the CHANGE\_MS\_POWER message or the  
CHANGE\_BS\_POWER message. After which in phase F34 the semaphore  
SEM\_RX is released and the program jumps to point B.
- 25 FIGS. 11 and 12 illustrate the subprogram LETMESS used for  
writing the MEASUREMENT\_RESULT message fields in external RAM  
respecting the image of FIG. 8. It is recalled that immediately  
before LETMESS there was performed the subprogram INDINAM which  
supplied the control point PG for choice of the external RAM page  
30 where there is allocated the 1024-word area reserved for the message  
to be processed and the address INTAB which indicates the beginning  
of said area in the memory page. The subprogram LETMESS comprises  
the following phases:
- a first phase M0 in which the DSP reads in DUAL.PORT.0 the fields  
35 DTX\_UL and DTX\_DL of the MEASUREMENT\_RESULT message, and in  
internal RAM the INTAB address;
- the following phase M1 is a test of the value of DTX\_UL; if the



- 47 -

- value is 0 it means that, as regards the present message, there has been no Discontinuous Transmission in the uplink direction and the program continues with phase M2 but otherwise jumps to phase M7;
- in phase M2 the DSP reads in DUAL.PORT.0 the present value of the two fields RXLEV\_FULL\_UP and RXQUAL\_FULL\_UP, then continues with phase M3;
  - in phase M3 the DSP reads in external RAM the words INBF\_LU and INBF\_QU which it will use in the following phase M4 to address the writing of the two fields just read in the respective sequences RXLEV\_FULL\_UP(1...32) and RXQUAL\_FULL\_UP(1...32).
  - In phase M4 the values of the fields RXLEV\_FULL\_UP and RXQUAL\_FULL\_UP are written in external RAM in the respective sequences. As regards the value RXLEV\_FULL\_UP, the write address is obtained by adding with INTAB a first fixed offset value by INTAB corresponding to the difference between the starting address of the subarea reserved for the homonymous sequence and the INTAB address itself, and to the two preceding terms is also added the present value of the word INBF\_LU. Perfectly dual addressing procedures apply for the value RXQUAL\_FULL\_UP, also in this case to INTAB is added a second fixed offset value whose meaning is like that of the first offset value, and to the two preceding terms is added the present value of the word INBF\_QU;
  - in the following phase M5 the values of INBF\_LU and INBF\_QU are written in the words DEBF\_LU and DEBF\_QU respectively; the latter will be used in phases F23 or F25 of the main program of the DSP to address reading of the terms of the RXLEV\_FULL\_UP(1...32) and RXQUAL\_FULL\_UP(1...32) sequences to calculate the means thereof. In this circumstance the read addresses are calculated in a manner similar to those of writing, substituting DEBF\_LU and DEBF\_QU for the words INBF\_LU and INBF\_QU;
  - in the following phase M6 the words INBF\_LU and INBF\_QU are increased by one modulus 32, so that at the next writing in the respective sequences the oldest value will be covered by the last. The covering process takes place continuously thanks to the increment modulus 32, in accordance with which the words INBF\_LU and INBF\_QU are zeroed when the value written is the 32nd or a multiple thereof; in this case the write addresses return to the

start of their respective sequences.

The instructions of the above phases justify what was said concerning the fact that, thanks to the words pairs used as modulus 32 counters associated with the 32-word sequences of FIG. 8, each sequence simulates a shift register. As regards the sequences considered thus far, the above said pairs of counters are represented by the word pairs INBF\_LU, DEBF\_LU and INBF\_QU, DEBF\_QU. The counters DEBF\_LU and DEBF\_QU count back from the value set in phase M5. Upon zeroing, the hexadecimal value 1F (decimal 31) is again set, and the back count continues until all 32 terms have been read and processed. Since in phase M6 the term from which back counting starts is shifted one position forward at each writing of a new term, the back reading of the sequence is equivalent to a shift of one position of all the terms of the sequence with expulsion of the oldest value and acquisition of the latest, as takes place in a shift register.

- Returning to the phase M1 test, if the answer reveals the presence of Discontinuous Transmission the program jumps to phase M7; the discussion of the following phases M7 to M11 is like that of the phases M2 to M6, but for the fields RXLEV\_SUB\_UL and RXQUAL\_SUB\_UL.
- Both phases M6 and M11 carry the program into phase M12; the discussion of the following phases M12 to M16 is like that of phases M2 to M6, but for the TIMING\_ADVANCE field with whose sequence are associated the words INBF\_TA and DEBF\_TA as modulus 32 counters.
- The following phase M17 is a test of the value of DTX\_DL; if the value is 0 it means that, as regards the present message, there was no Discontinuous Transmission in the downlink direction and the program continues with phase M18 but otherwise jumps to phase M23.
- The discussion of the following phases M18 to M22 is like that of phases M2 to M6 but for the fields RXLEV\_FULL\_DL and RXQUAL\_FULL\_DL with whose sequences are associated the words INBF\_LD and INBF\_QD respectively used as modulus 32 counters;
- if there is a jump to phase M23, the discussion of the following phases M23 to M27 is exactly like that of phases M18 to M22 but for fields RXLEV\_SUB\_DL and RXQUAL\_SUB\_DL.
- Both the phases M22 and M27 carry the program into phase M28 in

which is read in DUAL.PORT.0 the value of a pair of fields RXLEV\_NCELL\_(N), BSIC\_BCCH\_(N) and the value of the field No\_CELL, then the program goes into phase M29 in which is zeroed an index n used in the following phases;

- 5    - in the following phase M30 is completed a test on the bit b of the first word of the nth subtable and if bit b = 0 it means that the subtable is free and the program continues with phase M31 in which in the first word of the subtable in question is written the value of the field BSIC\_BCCH\_(N) giving value 1 to the related bit b;
- 10   - the discussion of the following phases M32 to M35 is exactly like that of phases M19 to M22 but for fields RXLEV\_NCELL\_(n) with whose sequences are associated the words INBF\_LD(n) and DEBF\_LD(n) used as modulus 32 counters;
- 15   - the following phase M36 is a test of the value of N to establish if it coincides with that of the field No\_CELL, whose value can vary from 0 to 6. If the answer is 'yes' it means that all the fields which are for the adjacent cells in the present MEASUREMENT\_RESULT message were acquired and written in external RAM, and in this case the subprogram terminates with an instruction to return to the main
- 20   program of the DSP. If the answer is 'no' there is a jump to phase M28 in which is read in DUAL.PORT.0 a new pair of fields RXLEV\_NCELL\_(N), BSIC\_BCCH\_(N) of the same message.
- 25   - Returning to the phase M30, if bit b = 1 it means that the nth subtable is occupied and in this case the program jumps to phase M37 in which the field BSIC\_BCCH\_(N) just read is compared with that contained in the first word of the nth subtable. If there is no coincidence between the two values, the program continues with phase M38 in which it increases the index n by one unit;
- 30   - the following phase M39 is a test of the index n to verify whether it has reached the value 16 corresponding to the maximum number of memorisable subtables. If n ≠ 16 there is a jump to phase M30 for repetition of the cycle consisting of phases M30, M37, M38 and M39 with increase of the index n at each comparison iteration.
- 35   - If the response to the M37 phase test is 'yes' it means that there is coincidence between BSIC\_BCCH\_(N) of the present message and the BSIC\_BCCH\_(n) written in the nth subtable during acquisition of the preceding messages. In other terms, the nth subtable is the one

reserved for the adjacent cell of index N. In this case the program jumps to phase M32 and performs phases M32 to M35 for writing of RXLEV\_NCELL\_(N) in the related RXLEV\_NCELL\_(n) sequence. The program enters then in phase M36 and continues in the manner described above.

- Returning to the phase M39 test, if  $n = 16$  it means that the BSIC\_BCCH\_(N) of the present message does not coincide with any of the BSIC\_BCCH\_(n) written in the 16 subtables during the preceding messages; in this case the program jumps directly to phase M36 ignoring the adjacent cell (N) and continues in the manner described above.

With reference to FIG. 13 there is now discussed a flow chart explaining in detail the processing performed in the individual phase F0 (FIG. 9) of the main DSP program. One of the purposes of said processing is to write in the internal RAM of the DSP the list of pointer tables of FIG. 7. It is also necessary to specify that the phase F0 is performed only upon starting the equipment and after each of hardware or software reinitialization of the DSP, and in particular after reception of the signal RESET-DSP.

The processing pertaining to this phase is described in the figures from the entirety of all the phases indicated by IN0 to IN33 in which:

- in phase IN0 are written in internal RAM all the E&M parameters necessary for the entirety of the processing performed by the DSP;
- in phase IN1 is written the value FRETAB00 in two registers of the DSP indicated by L and Q. As mentioned above, FRETAB00 represents the starting address in internal RAM of the list of tables of FIG. 7. The register Q is a register used by the DSP to generate the address for read and write access to its own internal RAM; specifically, the content of the register Q is said address;
- in phase IN2 an index I is zeroed and another address K set at hexadecimal value 0C00. The index I is used for counting the number of tables in the list; the function of the index K will be clarified below;
- in phase IN3 register Q is decreased by one unit to be able to address the word FRETABPTR which represents a pointer to the starting address of the first free table in the list which, in the

- 51 -

case of FIG. 7, is that pointed to by FRETAB00;

- in phase IN4 the content of register L, i.e. FRETAB00, is written in internal RAM at the FRETAPTR address; after which in phase IN5 register Q is increased by one unit and thus again contains the FRETAB00 value.

The following phases from IN6 to IN15 constitute a first write cycle of a first group of 50 tables which will be used for addressing as many 1024-word areas, allocated on page zero of the external RAM of the DSP to be assigned dynamically to the channels. Specifically:

- In phase IN6 with the pre-existing value of the index K is summed a hexadecimal value 0400. As can be seen from FIG. 7, with the first iteration of the write cycle the hexadecimal value reached by K is 1000;
- in phase IN7 the content of the register L is increased by 3 units and it will therefore contain the FRETAB01 value;
- in phase IN8 the content of L is written in internal RAM at the FRETAB00 address. Generalizing the remarks for phases IN6, IN7 and IN8 at all the iterations of the first write cycle, what is actually done is to write in the first word of the table being written the starting address of the following table;
- in phase IN9 the register Q is increased by one unit to address the second word of the table during the next write operation;
- in phase IN10 a word of all zeroes is written in internal RAM and there is thus placed at 0 also the bit which addresses the page 0 of the external RAM of the DSP;
- phase IN11 is like phase IN9;
- in phase IN12 the present value of the index K is written in internal RAM in the third word of the table being written.

It is useful to recall that the third word of each table contains a respective external RAM address which in page 0 or 1 marks the start of a 1024-word area which will be assigned dynamically to the channels; this area is therefore constantly associated with the respective table. The increase of hexadecimal 0400 of the index K (corresponding to an increase of 1024 decimal) prepares for writing in the next table of the starting address list of the following external RAM area;

- 52 -

- phase IN13 is the same as phases IN9 and IN11;
- in phase IN14 index I is increased by one unit and in phase IN15 a test of index I is completed to see if the 50th table was also written in internal RAM; if not, there is a jump to the start of phase IN6 for repetition of the cycle IN6 to IN15 but otherwise the program continues with phase IN16 in which index I is zeroed and index K reinitialised at hexadecimal value 0C00.
- The following phases from IN17 to IN26 constitute a second write cycle of a second group of 50 tables, which will be used to address as many 1024-word areas placed in page 1 of the external RAM of the DSP to be assigned dynamically to the channels. The processing completed in the cycle IN17 to IN26 is like that for the cycle IN6 to IN15 to the description of which reference is made. The only differences between the two cycles consist of the fact that, as regards the cycle IN17 to IN26, in the second words of the tables all the bits are written with value 1, and hence even the bit used for addressing page 1 of the external RAM is 1; and the fact that in the phase IN26 test it is asked if index I has reached the value 49 corresponding to the 99th and penultimate table. If it has, the second write cycle also terminates and the program enters phase IN27;
- phase IN27 is like phases IN6 and IN17;
- in the following phase IN28 is written in the first word of the 100th and last table a hexadecimal value FFFF, which no longer represents a pointer to the following table but rather indicates that there are no more external RAM areas available for the channels;
- the following phases IN29 to IN32 are exactly like phases IN20 to IN23 to whose description reference is made;
- the last phase IN33 corresponds to a zeroing of the external RAM of the DSP, after which there is a jump to point B of the main program of the DSP (FIG. 9).

With reference to FIG. 14 there is now described the subprogram INDINAM whose primary purpose is to give the address of a 1024-word area of external RAM, presently free, to be assigned to the channel indicated in a MEASUREMENT\_RESULT message acquired for the first time from the DSP. The processing completed in the various phases of

- 53 -

INDINAM is as follows:

- in phase D0 are read in DUAL.PORT.0 the fields D, TEI and CHANNEL\_NBR;
- in phase D1 are appropriately decoded the 11 bits of the fields  
5 just read to find an address CHAN\_ADR of a word allocated in the initial 2048-word area of the external RAM of the DSP (area PTR of FIG. 8);
- in phase D2 is transcribed in a register ACC0 the external RAM address word CHAN\_ADR; said word is made up of two fields. i.e. the  
10 bit a, and a pointer indicated by FRETABXY which represents one of the 100 possible pointers FRETAB00 to FRETAB99 of FIG. 7. These fields are initially at value zero and will be filled during operation of the system in the manner described below;
- in phase D3 is completed a test of the value of the bit a, and if  
15 it is 1 it means that the area reserved for the channel had already been assigned and in this case the program continues with phase D4 in which is transcribed in the register Q the field FRETABXY contained in ACC0; the function of the register Q was clarified during the discussion of FIG. 13;
- in the following phase D5 the content of the register Q is  
20 increased by one unit to prepare the address of the second word of the present internal RAM table pointed to by FRETABXY which contains the address bit of page zero or one of external RAM;
- the program then enters phase D6 in which it reads said page bit  
25 and in phase D7 it uses it to command writing of the corresponding control point PG in the register SC.REG (FIG. 3);
- the following phase D8 is like D5 but in this case it serves to prepare the address of the third table word which contains the starting address, inside the page, of the external RAM area  
30 associated with the table;
- in the following phase D9 the third word is read in internal RAM (see last phase) and memorized in a register INTAB;
- after which in the phase D10 there is a return to the main program where is transferred the content of the register INTAB to be used  
35 by the program and by the subprogram LETMESS in the manner described above.

In view of the foregoing, it can be noted that the search in external

RAM of the area assigned to the present channel does not take place from mere decoding of the MEASUREMENT\_RESULT message fields which identify the channel but passes through the addressing tables of FIG. 7. It is just this passing through which allows dynamic assignment, as will be seen presently.

- Returning to the test on the bit a of phase D3 left in suspense, if the value read is zero it means that to the channel in question has not yet been assigned a 1024-word area in external RAM, and in this case the program jumps to phase D11 for the related assignment;
- 10 - in phase D11 is transcribed the address of FRETABPTR (FIG. 7) in the register Q;
- in the following phase D12 FRETABPTR is read in internal RAM and transcribed in the register ACC0, which now thus contains the starting address of the first 'free' table in the list of FIG. 7;
- 15 - the following phase D13 is a test of the value of ACC0 to establish whether it is equal to the hexadecimal value FFFF, and if it is it means that the 100 areas of external RAM have all been assigned, and in this case the program jumps to point B for reading of another message, ignoring the present message which is lost.
- 20 - But if in phase D13 the value of FRETABPTR is different from FFFF it means that there are still areas available and the program goes into phase D14 in which the content of ACC0, i.e. the FRETABPTR, is transcribed in external RAM in the address word CHAN\_ADR, and specifically in the field FRETABXY thereof;
- 25 - in the following phase D15 the bit a is written to value 1 of said word to signal that an area for processing of the channel in question has been temporarily assigned, after which the program in the following phases from D16 to D19 updates in internal RAM the value of FRETABPTR, since the table of FIG. 7 which was formerly
- 30 free is now engaged.  
Specifically:
- in phase D16 the content of the register ACC0, i.e. the pointer FRETABPTR which pointed to the internal RAM table just engaged, is transcribed in register Q in order to address the first word of
- 35 said table;
- in phase D17 the first word of said table is read and transcribed in a register ACC1, which thus contains the new pointer to the next



free table in the list;

- phase D18 is like D11 and serves to prepare the FRETABPTR address;
- in phase D19 the content of ACC1 is transcribed in FRETABPTR which is thereby updated;

- 5
- the next phase D20 is like D16 and produces the same effects, the value contained in ACC0 not being changed at the same time;
  - at this point the program jumps to the start of phase D5 and performs in succession phases D5 to D10 described above.

With reference to FIG. 15 there is now described the subprogram

- 10
- RILCAN whose purpose is to release a 1024-word area of external RAM presently occupied because there has arrived a RESET message regarding the channel which occupies this area. The processing completed in the various phases of RILCAN are as follows:

- 15
- phases R0, R1, R2 and R3 are identical with phases D0, D1, D2 and D3 respectively of the preceding subprogram INDINAM, to which reference is made for the description. In particular, in phase R2 the word read in external RAM at the CHAN\_ADR address comprises certainly the bit a and the FRETABXY field because the subprogram operates on an area already assigned.

- 20
- The test on the bit a of phase R3 is completed anyway, despite the previous statement, to protect against possible errors of the system software which could erroneously address a RESET message to an unassigned memory area. In this case the subprogram immediately returns into the main program without performing any processing.

- 25
- In the more general case, the subprogram passes instead from phase R3 to phase R4; all the following phases up to the return instruction are performed without program jumps and therefore the sequential order of the instructions also respects the order of execution thereof.

- 30
- in the phase R4 is transcribed the FRETABPTR address (FIG. 7) in register Q; the function of this register was explained during the discussion of FIG. 13;

- in phase R5 the value of FRETABPTR is read in internal RAM and memorized in a register ACC1;

- 35
- in phase R6 is transcribed in register Q the FRETABXY field contained in ACC0;

- in phase R7 the content of ACC1, i.e. FRETABPTR, is written in

internal RAM.

What is actually done in phases R4 to R7 is transcription of FRETABPTR in the first FRETABXY address word of the table of FIG. 7 to be made newly available.

5 - In phase R8 the FRETABPTR address is copied again in the register Q; and

- in phase R9 the FRETABXY field is written in internal RAM.

With the processing of the two above phases the FRETABPTR is updated and now contains the FRETABXY address of the first word of said table  
10 which now becomes the first free table of the list.

Processing of the following phases R10 to R14 allows obtaining the control point PG within the external RAM page of the 1024-word area which must be freed. Said phases are identical to those indicated by D5 to D9 in the subprogram INDINAM with the only  
15 difference that the address of the 1024-word area is now indicated by TABRIL, and that in phase R10 register Q is increased by two units instead of one.

- In phase R15 the address word CHAN\_ADR is zeroed in external RAM;  
- In phase R16 the external RAM area addressed by TABRIL is zeroed,  
20 after which there is a return into the main program.

Thanks to the above detailed discussion of the flow charts of FIG. 4, FIGS. 9 to 15 and the memory charts of FIGS. 7 and 8 and using the information available in the operating and programming manuals of the microprocessors indicated, or equivalent, and those of the GSM  
25 specifications from time to time indicated, one skilled in the art of microprocessors can provide the governing programs of the processing units included in the processor of telephone signaling originated by transmission measurements which are the object of the present invention.

30 From the sum of the above considerations on the software governing the operation of the CPU and the DSP there emerges another advantage and specifically that of the opportuneness of the processor in question in suiting its operational decisions to the short-term variations of the transmission conditions. Indeed, said decisions  
35 are updated every 480ms.

## CLAIMS

1. Processor of telephone signaling generated by transmission measurements (PPLD) for digital mobile radio systems belonging to a control apparatus (BSC) of multiple fixed radio stations (BTS) located in respective territorial cells and comprising transceivers in connection with mobile telephone equipments (MS) to which are assigned respective communication channels subject to Handover; said control apparatus (BSC) being in communication with the fixed radio stations (BTS) by means of first numerical flows (1) and with a mobile radio system switching station (MSC) and an operation and maintenance center by means of second numerical flows (2); said first and second numerical flows consisting of bit sequences in recognizable and numbered serial frames divided in traffic and signaling channels, the signaling channels carrying telephone messages comprising control fields and 'informative contents' underlying a communication protocol with multiple hierarchical levels; said control apparatus (BSC) comprising also: a processor dedicated to management of the radio resources (TDPC) on the basis of the mobility of users which is connected to said telephone signaling processor generated by transmission measurements (PPLD) and to a peripheral interface processor (PPCC) to said second numerical flows (2); an administrative processor (MPCC) which carries out functions of supervision and maintenance of the control apparatus (BSC) and of the fixed radio stations (BTS) and is connected to each of said processors; first means (OTLP, SN64) which extract from said first numerical flows (1) the respective signaling channels and convey them to said processor of telephone signaling generated by transmission measurements (PPLD), and which insert in said first numerical flows (1) the signaling channels from said processor; second means (OTLP, SN64) which extract from said second numerical flows (2) the respective signaling channels and convey them to said peripheral interface processor and vice versa, characterized in that it comprises furthermore:

a first processing unit (80C186.CIRCUITS) substantially consisting of a first processor connected to a RAM of its own, to a first interface (SN64.INT) to said first means (SN64, OTLP) which extract/insert the signaling channels from/into said first

numerical flows, and additionally connected to a second interface (DUAL.PORT.1, TDPC.INT) to said processor dedicated to the management of the radio resources (TDPC), and to a third interface (MPCC.INT) to said administrative processor (MPCC); said first  
5 processor receiving messages through said interfaces, recognizing the start of a valid message and memorizing it, checking and restoring the integrity of the bits of the message received, checking that the order of arrival of successive valid messages corresponds to that of a correct sequence, asking for  
10 retransmission of missing messages and restoring said correct sequence, copying the 'informative contents' of said valid messages in a first Dual Access RAM (DUAL.PORT.0) when said 'informative contents' are substantially for transmission measurements concerning power values and quality of the radio signal and of  
15 distance between connected points, and sending additional valid messages which do not concern said transmission measurements to corresponding address members (BTS, MS; TDPC, MSC) by means of the respective said interfaces (SN64.INT, DUAL.PORT.1, TDPC.INT);  
a second processing unit (DSP.CIRCUITS) substantially  
20 consisting of a second processor (DSP16A) particularly oriented to performance of arithmetical operations in real time, which reads from said first Dual Access RAM (DUAL.PORT.0) said 'informative contents' and writes them in areas of a RAM of its own RAM, dynamically assigned, to execute thereon appropriate processing and  
25 taking 'processed messages' comprising indications for performance of said Handovers and for checking the transmitting power of the transmitters included in said mobile telephones (MS) or in said fixed radio stations (BTS), said 'processed messages' being copied in said first Dual Access RAM (DUAL.PORT.0);  
30 and in that said first processor reads from said first Dual Access RAM (DUAL.PORT.0) said 'processed messages' to which it adds additional control fields to obtain complete messages which it sends, through said interfaces, to said processor dedicated to management of the radio resources (TDPC), to said transceivers  
35 belonging to said fixed radio stations (BTS), to said mobile telephones (MS), and to said switching station for mobile radio systems (MSC).

2. Processor of telephone signaling generated by transmission measurements in accordance with claim 1, characterized in that:

5 said first Dual Access RAM (DUAL.PORT.0) possesses a first access port connected to the bus of said first processor (80C186) for read and write operations, and a second access port connected to the bus of said second processor (DSP16A) for read and write operations;

10 said first processor (80C186) prepares in the first Dual Access RAM (DUAL.PORT.0) a first memory zone in which to store a queue of messages to be sent to said second processor (DSP16A), and a second memory zone in which said second processor (DSP16A) stores a queue of messages to be sent to said first processor (80C186), said messages being inserted in the respective queues respecting the time order in which they are acquired, or generated, and being  
15 taken in an order of decreasing priority which assigns the highest priority to the oldest message in the queue; and

20 said first and second memory zones reserved for storage of said queues possess respective programmable means designed to govern the read and write accesses by said first (80C186) and second (DSP16A) processor.

3. Processor of telephone signaling generated by transmission measurements in accordance with claim 1, characterized in that said first interface (SN64.INT) comprises:

25 demultiplexers of signaling channels carried by entering serial signaling flows (2MSN.IN) generated by said first means (SN64.OTLP) which extract said signaling channels from said first numerical flows (1) and insert them appropriately in said entering serial signaling flows (2MSN.IN);

30 serial communication devices designed to receive messages in serial form from the demultiplexed signaling channels (LAPD.LK.IN) from said entering serial signaling flows (2MSN.IN), and to transfer said messages in parallelized form to said first processor and to receive messages in parallelized form from said first processor and convert said messages in serial form transferring  
35 them to outgoing signaling channels (LAPD.LK.OUT);

multiplexers of said outgoing signaling channels (LAPD.LK.OUT) in outgoing serial signaling flows (2MSN.OUT)

directed to said first means (SN64,OTLP) which insert appropriately said outgoing signaling channels in said first numerical flows (1).

4. Processor of telephone signaling generated by transmission measurements in accordance with claim 1 characterized in that:

said second interface (DUAL.PORT.1,TDPC.INT) comprises a second Dual Access RAM (DUAL.PORT.1) which possesses a first access port connected to the bus of said processor dedicated to the management of the radio resources (TDPC) for the related read and write operations, and a second access port connected to the bus of said first processor (80C186) for the related read and write operations;

said first processor (80C186) prepares in the second Dual Access RAM (DUAL.PORT.1) a third memory zone in which to store a queue of messages to be sent to said processor dedicated to the management of the radio resources (TDPC) and a fourth memory zone in which said processor dedicated to the management of the radio resources (TDPC) stores a queue of message to be sent to the first processor (80C186), said messages being inserted in the respective queues respecting the time order in which they are acquired, and being taken in decreasing order of priority which assigns the highest priority to the oldest message in the queue; and

said third and fourth memory zones reserved for storage of said queues possess respective programmable means designed to govern their read and write accesses by said first processor (80C186) and by said processor dedicated to the management of the radio resources (TDPC).

5. Processor of telephone signaling generated by transmission measurements in accordance with claim 1, characterized in that said second processor (DSP16A) performs a processing initialization phase (F0) of the content of said own memory RAM, mainly upon starting and after each reinitialization, and a following processing cycle iterated indefinitely; said initialization phase (F0) comprising the following steps:

- 11) writing of some parameters (E&M) necessary for the subsequent processing in a first zone of said own memory RAM;
- 12) writing of a list including a number M of tables in a second zone of said own memory RAM, said tables being utilized in

5 said dynamic assignment of areas (CELL.SER, CELL.AD) of said own memory RAM to the 'informative contents' of said signaling channels; said number M being lower than the number of said signaling channels, and being evaluated with criteria dependent upon the telephone traffic existing in the territory served by said control apparatus (BSC) of the fixed radio stations (BTS);

- 10 13) zeroing of a third zone of said own memory RAM reserved for memorization of 'channel words' designed to set a linked, or not linked, status of said M tables to said signaling channels;
- 15 14) zeroing of a fourth zone of said own memory RAM optionally divided in two or more memory partitions reserved to said areas to be dynamically assigned to the signalling channels; each iteration of said processing cycle performed indefinitely comprising the following processing phases performed in chronological order:

- 20 a) reading in said first Dual Access RAM (DUAL.PORT.0) of a first and second field (MESSAGE\_TYPE; D,TEI,CHANNEL\_NBR) belonging to said 'informative contents' of a higher-priority message, said first field (MESSAGE\_TYPE) being designed to identify the message type to be processed (MEASUREMENT\_RESULT, MS\_RF\_POWER\_CAPABILITY, HO\_CANDIDATE\_ENQUIRE\_INVOKE, RESET), said second field
- 25 (D,TEI,CHANNEL\_NBR) identifying a signaling channel with which is associated said message to be processed;
- b) analysis of said first field (MESSAGE\_TYPE) and identification of the message type;
- 30 c) possible 'dynamic' assignment of one of said M memory areas (CELL.SER, CELL.AD) to one signaling channel identified by said second field (D,TEI,CHANNEL\_NBR) for the duration of a communication served by said channel;
- 35 d) reading in said first Dual Access RAM (DUAL.PORT.0) of remaining third fields of said 'informative contents' comprising essentially transmission measurements values, and writing of the same in said area assigned dynamically to said channel;

- e) performance of said appropriate processing concerning said remaining third fields of said 'informative contents' and obtaining of said 'processed messages', the appropriate processing depending on the preceding message type identification;
- 5 f) writing of said 'processed messages' in said first Dual Access RAM (DUAL.PORT.0);
- g) unconditional jump to the first phase a) of the processing cycle consisting of the preceding phases (a to g) and repetition of said cycle during subsequent iterations of said processing cycle and there being read and processed
- 10 'informative contents' of subsequent messages memorized in priority order.

6. Processor of telephone signaling generated by transmission measurements in accordance with claim 5, characterized in that:

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in the fourth phase (d) of said processing cycle the remaining third fields of said 'informative content' written in said area assigned to said channel are written in respective sequences of K values for each third field, with K preferable equal to 32, said sequences being allocated in adjacent memory zones and constituting a succession of sequences;

20

said remaining third fields processed in the fifth phase (e) of said processing cycle contain values of respective transmission measurements (RXLEV\_FULL/SUB)\_UL, RXQUAL\_(FULL/SUB)\_UL, RXLEV\_(FULL/SUB)\_DL, RXQUAL\_(FULL/SUB)\_DL, TIMING\_ADVANCE) for a 'serving' cell with which a generic mobile telephone is affiliated, and transmission measurement values (REXLEV\_NCELL\_(n)) for a number n of adjacent cells; said appropriate processing comprising operations of means performed on the terms of each said sequence of K values, and

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in the sixth phase (f) of said processing cycle are written in said first Dual Access RAM ((DUAL.PORT.0) first 'processed messages' (CHANGE\_MS\_POWER, CHANGE\_BS\_POWER) for control of the transmission power of the fixed or mobile sets, or second 'processed messages' (CONDITION\_FOR\_INTER\_CELL\_HO, CONDITION\_FOR\_INTRA\_CELL\_HO) comprising indications for performance of the Handovers.

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7. Processor of telephone signaling generated by transmission measurements in accordance with claim 6, characterized in that the updating of said sequences executed in said fourth phase (d) of said processing cycle includes the following steps performed in chronological order (LETMESS):

- 5 d1) reading of a said third field of said 'informative content';
- d2) generation of a write address of said third field in a respective sequence of K values, the write address being calculated by adding with the start address (INTAB) of said  
10 memory area assigned to said channel, a respective offset value corresponding to the difference between a start address of said respective sequence and a start address of a first sequence of said succession of sequences, and also adding to the two preceding terms a count value reached by a K modulus  
15 forward counter located at the tail of said respective sequence and associated therewith;
- d3) writing of said third field in a word of said respective sequence whose address is calculated in the preceding step (d2);
- 20 d4) initialization of a K modulus back counter associated with said respective sequence with the count value currently reached by said K modulus forward counter;
- d5) modulus K increase of said forward counter;
- 25 d6) verification of the existence of additional sequences to be updated and, if affirmative, repetition of the preceding steps d1 to d6 for another sequence to be updated; otherwise, unconditional jump to the end of said fourth phase (d) of said processing cycle.

8. Processor of the telephone signaling generated by  
30 transmission measurements in accordance with claim 6, characterized in that said appropriate processing executed in the fifth phase (e) of said processing cycle consists principally of the following operations:

- 35 e1) choice of a type of mean to be used in the following operations;
- e2) execution of said chosen mean on each of said respective sequences of K values;

- e3) comparison of means obtained as set forth in the above point e2), for particularly significant sequences as concerns control of the transmission power (RXLEV\_FULL/SUB)\_UL, RXQUAL\_(FULL/SUB)\_UL, RXLEV\_(FULL/SUB)\_DL, RXQUAL\_(FULL/SUB)\_DL, with a first group of thresholds having preset values, obtaining first criteria directly usable for the generation of a first 'processed message' (CHANGE\_MS\_POWER, CHANGE\_BS\_POWER);
- e4) evaluation of said first criteria and optional execution of said sixth phase (f) of said processing cycle, otherwise jump to a subsequent phase e5);
- e5) comparison of means obtained in accordance with the above point e2), for particularly significant sequences as concerns management of the Handover operations (RXLEV\_FULL/SUB)\_UL, RXQUAL\_(FULL/SUB)\_UL, RXLEV\_(FULL/SUB)\_DL, RXQUAL\_(FULL/SUB)\_DL, TIMING\_ADVANCE, REXLEV\_NCELL\_(n)), with a second group of thresholds having preset values, obtaining second criteria usable for generation of a said second 'processed message';
- e6) calculation of appropriate merit parameters (POWER BUDGET) related to the quality of the radio connection between a mobile telephone and a group of adjacent cells;
- e7) comparison of said merit parameters with a respective third group of thresholds having preset values and taking third criteria (HO\_MARGIN(n)) usable for generation of said second 'processed message';
- e8) compilation of a list of preferred adjacent cells arranged in order of priority as concerns execution of a Handover operation on the basis of said first, second and third criteria;
- e9) evaluation of said first, second and third criteria and generation of said second 'processed message' (CONDITION\_FOR\_INTER\_CELL\_HO, CONDITION\_FOR\_INTRA\_CELL\_HO) comprising indications for execution of a Handover, among whose indications is comprised said list of preferred adjacent cells;
- e10) execution of said sixth phase (f) of said processing cycle.

9. Processor of telephone signaling generated by transmission measurements in accordance with claim 7, characterized in that said respective K module back counter supplies values for calculation of K addresses of generic terms in a respective sequence for processing thereof.

10. Processor of telephone signaling generated by transmission measurements in accordance with claim 5, characterized in that each table belonging to said list of M tables written in said second memory zone during said initialization phase (FO) comprises the following memory words:

- a first word in which is written an initial address of another table which is in sequential position in said list, said additional table is concatenated with the preceding table by means of said initial address, having pointer functions (FETABXY, 00...99);
- a second word containing a third field used for addressing said partitions of said fourth memory zone (RAM);
- a third word in which is memorized an initial address (1000H...D400H) of a said memory area to be assigned dynamically to the channels inside a generic partition and, only in the case of a last Mth table of the list, an indicator (FFFFH) of the lack of further memory areas (RAM) to be assigned to the channels;

also characterized in that with the list of tables is associated an additional pointer (FRETABPTR) indicating the start of a first free table of the list, being considered free a table which is not linked to any signaling channel by means of a respective said 'channel word'; said table list being used in the third phase c) of said processing cycle to assign a memory area to a signaling channel identified by said second field (D,TEI,CHANNEL\_NBR), or for release of said area in case said first field identifies a release message (RESET) of the signaling channel resources, the area released remaining available for a subsequent reassignment to a different channel or optionally to the same one.

11. Processor of telephone signaling generated by transmission measurements in accordance with claim 10, characterized in that the third phase c) in which a said memory area is assigned 'dynamically' to a signaling channel includes the following

processing steps performed in chronological succession (INDINAM):

- c1) decodification of said second field (D,TEI,CHANNEL\_NBR) and generation of a read address (CHAN\_ADR) of a 'channel word' and reading thereof;
- 5 c2) decodification of the logic state of a fourth field (a) included in the 'channel word', containing indications on the linkage or non-linkage state of said table of the list with the signaling channel identified by said second field (D,TEI,CHANNEL\_NBR) and, in case of non-linkage, execution of  
10 six processing steps (c3...c8) immediately sequential to the step currently being performed (c2) but, in case of linkage, execution of a jump of said six sequential steps and execution of remaining sequential steps;
- 15 c3) reading of said additional pointer (FRETABPTR) indicating a first free table of the list and unconditional jump to the end of said third phase (c) when the value read (FFFFH) corresponds to that of said indicator of lack of additional memory areas (RAM) to be assigned to the channels, otherwise continuation in sequence;
- 20 c4) writing of said additional pointer (FRETABPTR) in a fifth field (FRETABXY) belonging to said 'channel word' and concomitant writing in said fourth field (a) of the same word, of a logical value indicating completed state of linkage to said signaling channel of said first free table of the list;
- 25 c5) reading of a said first word (FRETABXY) belonging to the table addressed by said additional pointer (FRETABPTR) and replacement of said additional pointer (FRETABPTR) by said first word read (FRETABXY);
- 30 c6) reading of a said second word belonging to the table addressed by said additional pointer (FRETABPTR), decodification of said third field and selection of a partition of said fourth memory zone (RAM);
- 35 c7) reading of said third word belonging to the table addressed at the preceding step (c6) and writing of the third word in a first register used to generate a start address (INTAB) of said memory area assigned to the channel in said selected partition;

c8) unconditional jump to the end of said third phase (c) of said processing cycle;

execution of the following steps, after step c2, as an alternative to steps c3 to c8:

- 5 c9) reading of a fifth field (FRETABXY) belonging to said 'channel word' and use of the value read as pointer to a table of the list previously assigned to said signaling channel;
- c10) reading of said second word belonging to the table assigned to the channel, decodification of said third field and selection  
10 of a respective partition of said fourth memory zone (RAM);
- c11) reading of said third word belonging to the table assigned to the channel and writing of said third word in a first register used to generate a start address (INTAB) of said memory area assigned to said channel in said selected partition; and
- 15 c12) unconditional jump to the end of said third phase (c) of said processing cycle.

12. Processor of the telephone signaling generated by transmission measurements in accordance with claim 11,  
characterized in that said third phase (c) in which said memory  
20 area assigned to said channel must be released also comprises the following processing steps (RILCAN) performed in chronological succession:

- 25 r1) decodification of said second field (D,TEI,CHANNEL\_NBR) for generation of an address (CHAN\_ADR) of a said 'channel word' and reading thereof;
- r2) reading of said pointer (FRETABXY) memorized in said fifth field of the 'channel word';
- r3) writing of said additional pointer (FRETABPTR) indicating a first free table of the list in said first word of a said  
30 table addressed by said pointer (FRETABXY) read in said fifth field of the 'channel word';
- r4) replacement of said additional pointer (FRETABPTR) indicating a first free table of the list by said pointer (FRETABXY) read in said fifth field of the 'channel word';
- 35 r5) reading of said second word belonging to the table addressed at the preceding step r3), decodification of said third field and selection of a respective partition of said fourth memory

- zone (RAM) in which is allocated a said area to be released;
- 5      r6) reading of said third word belonging to the table addressed in the preceding step r3) and writing of said third word in said first register used for generating a start address (TABRIL) of said area which must be released;
- r7) release of said area which must be released by zeroing it;
- r8) writing in said fourth field (a) of said 'channel word' of a logical value indicating the state of non-linkage of said table addressed to the preceding step r3) with said released area, and
- 10      r9) unconditional jump to the end of said third phase (c) of said processing cycle.

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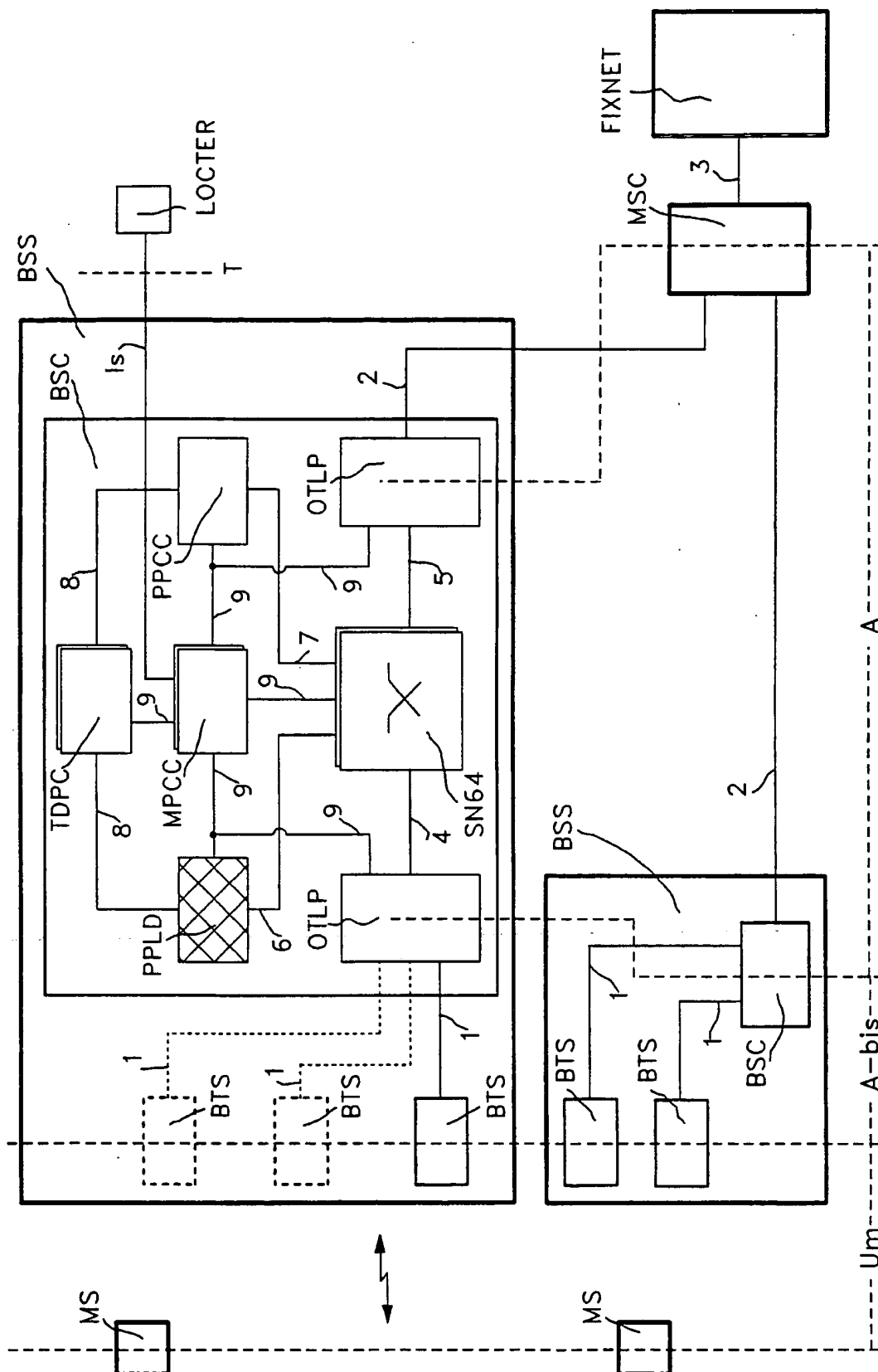


FIG. 1

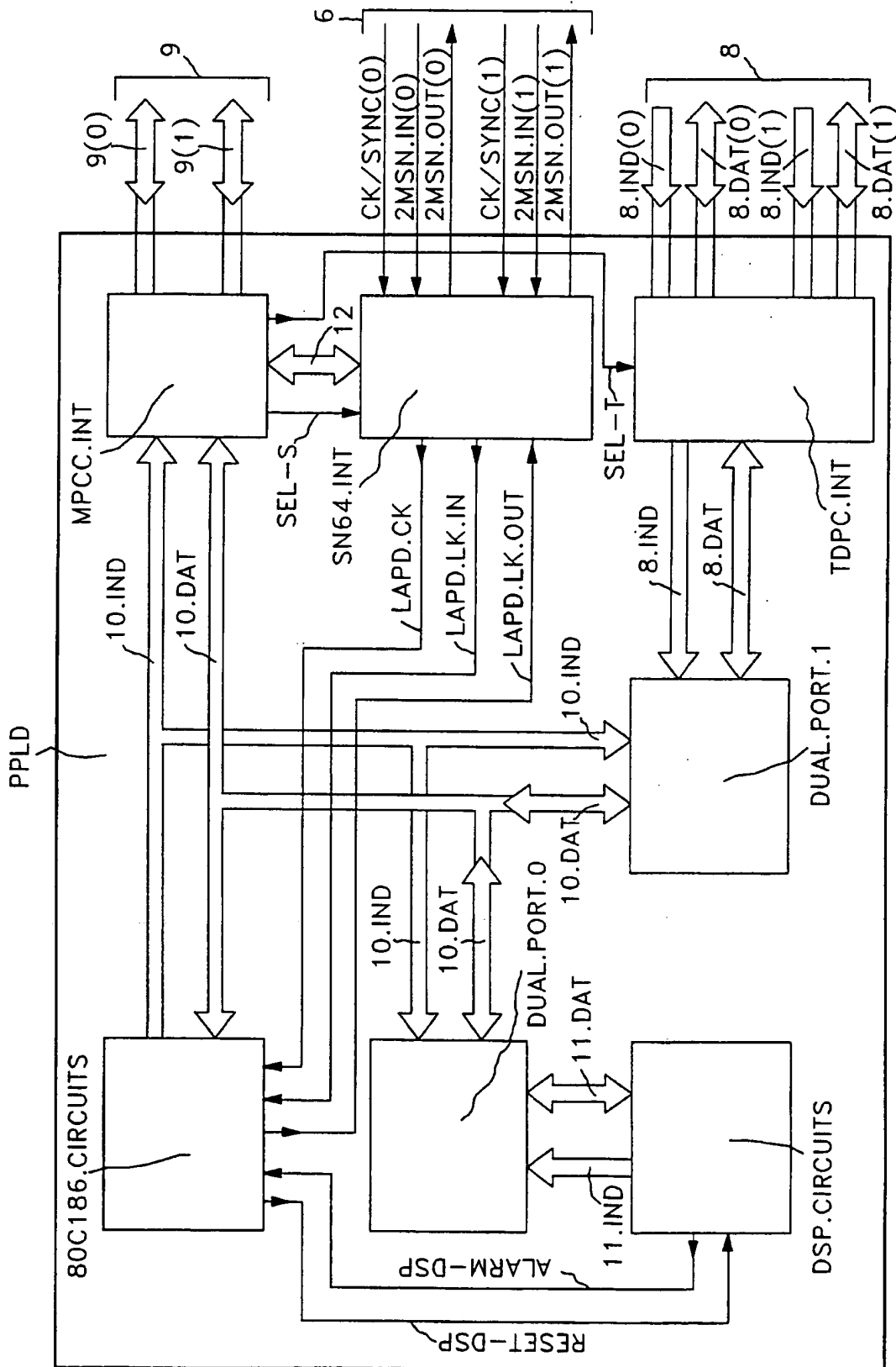


FIG. 2



4/14

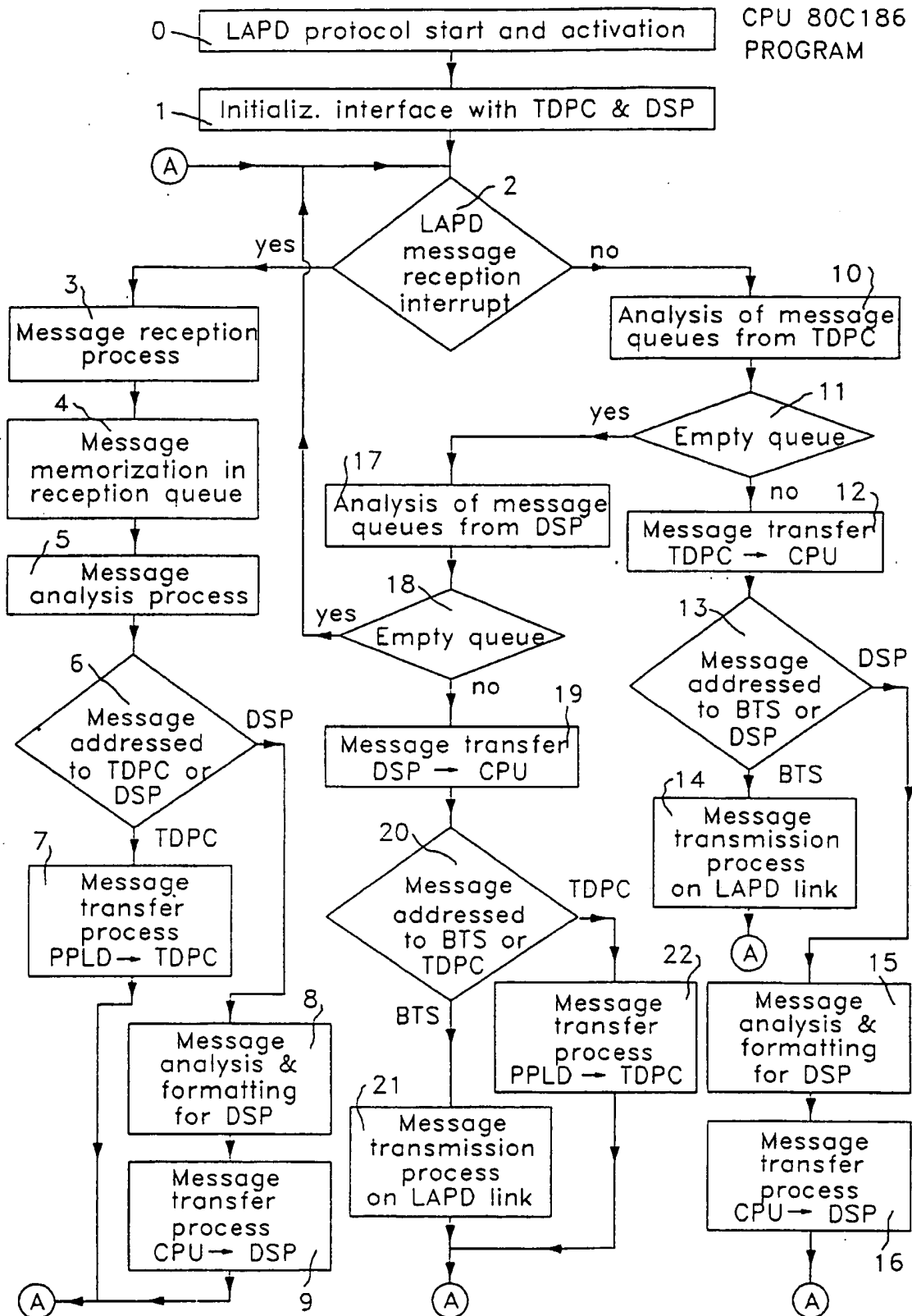


FIG. 4

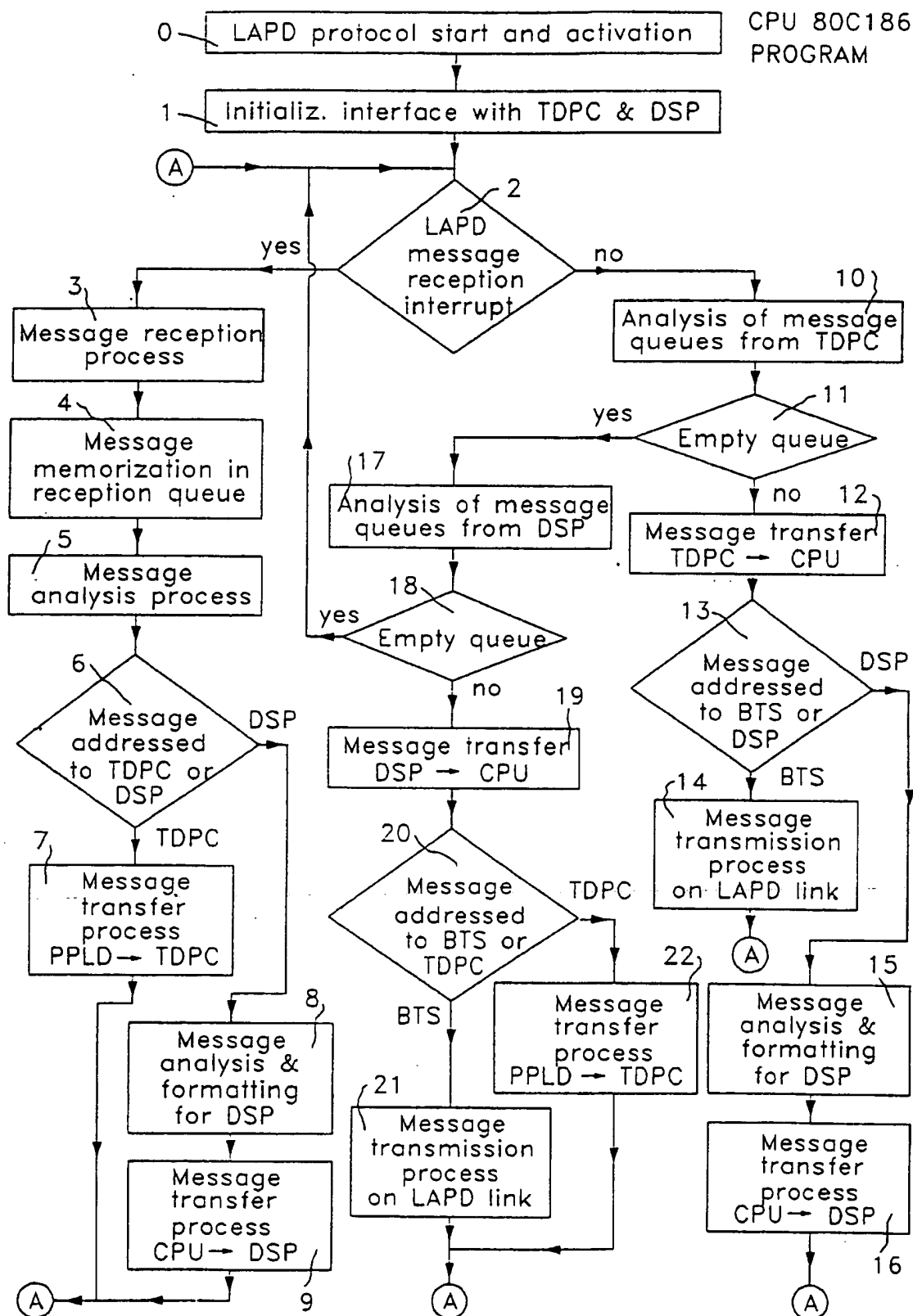


FIG. 4

5/14

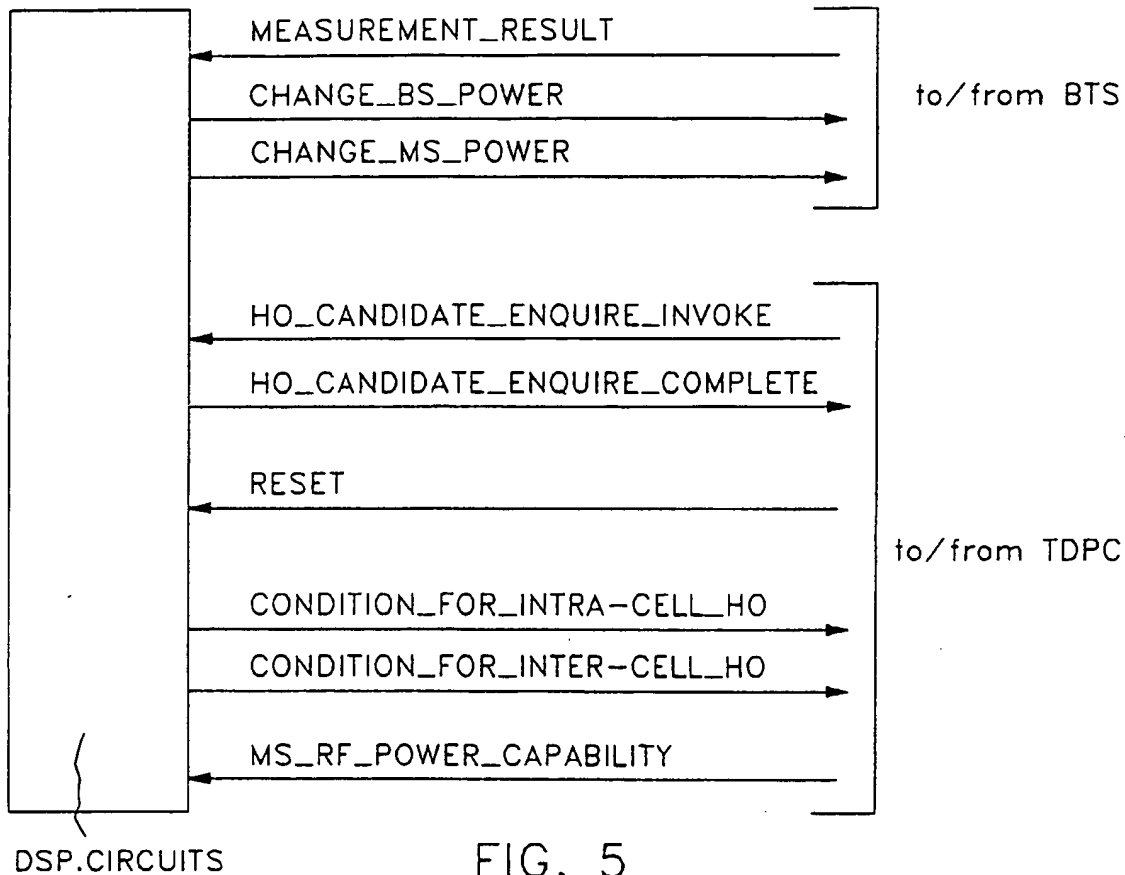


FIG. 5

MESSAGE_TYPE		
D	TEI	CHANNEL_NBR
DTX_DL		
RXLEV_FULL_DL		
RXLEV_SUB_DL		
RXQUAL_FULL_DL		
RXQUAL_SUB_DL		
DTX_UL		
RXLEV_FULL_UP		
RXLEV_SUB_UP		
RXQUAL_FULL_UP		
-----		

measurements  
by MS

measurements  
by BTS

FIG. 6a

6/14

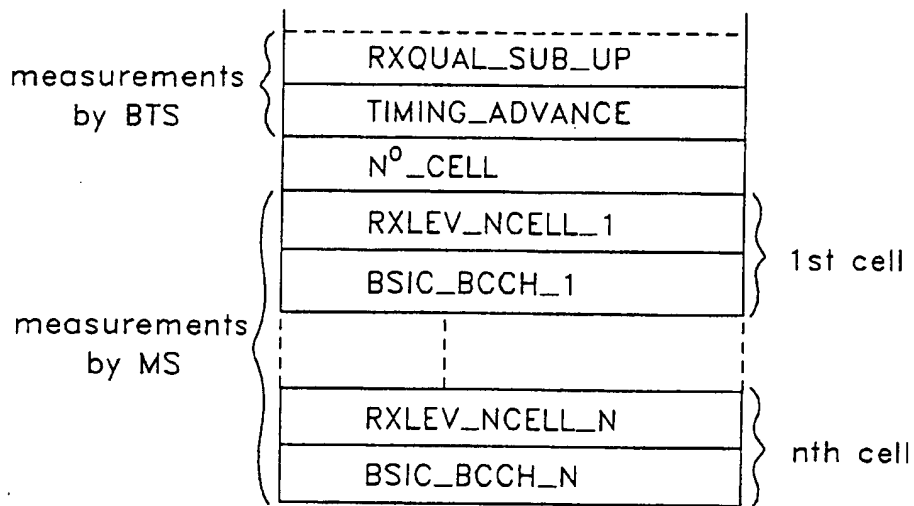


FIG. 6b

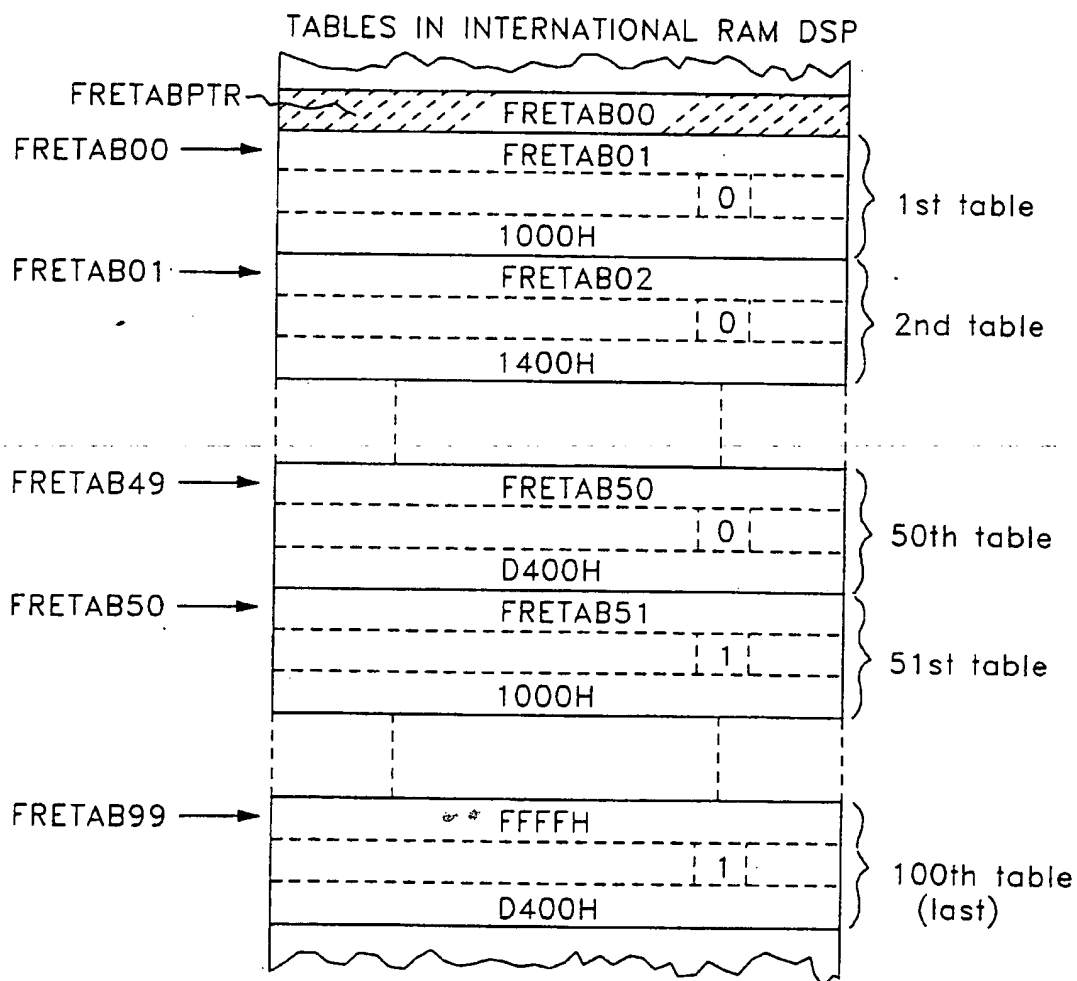


FIG. 7

7/14

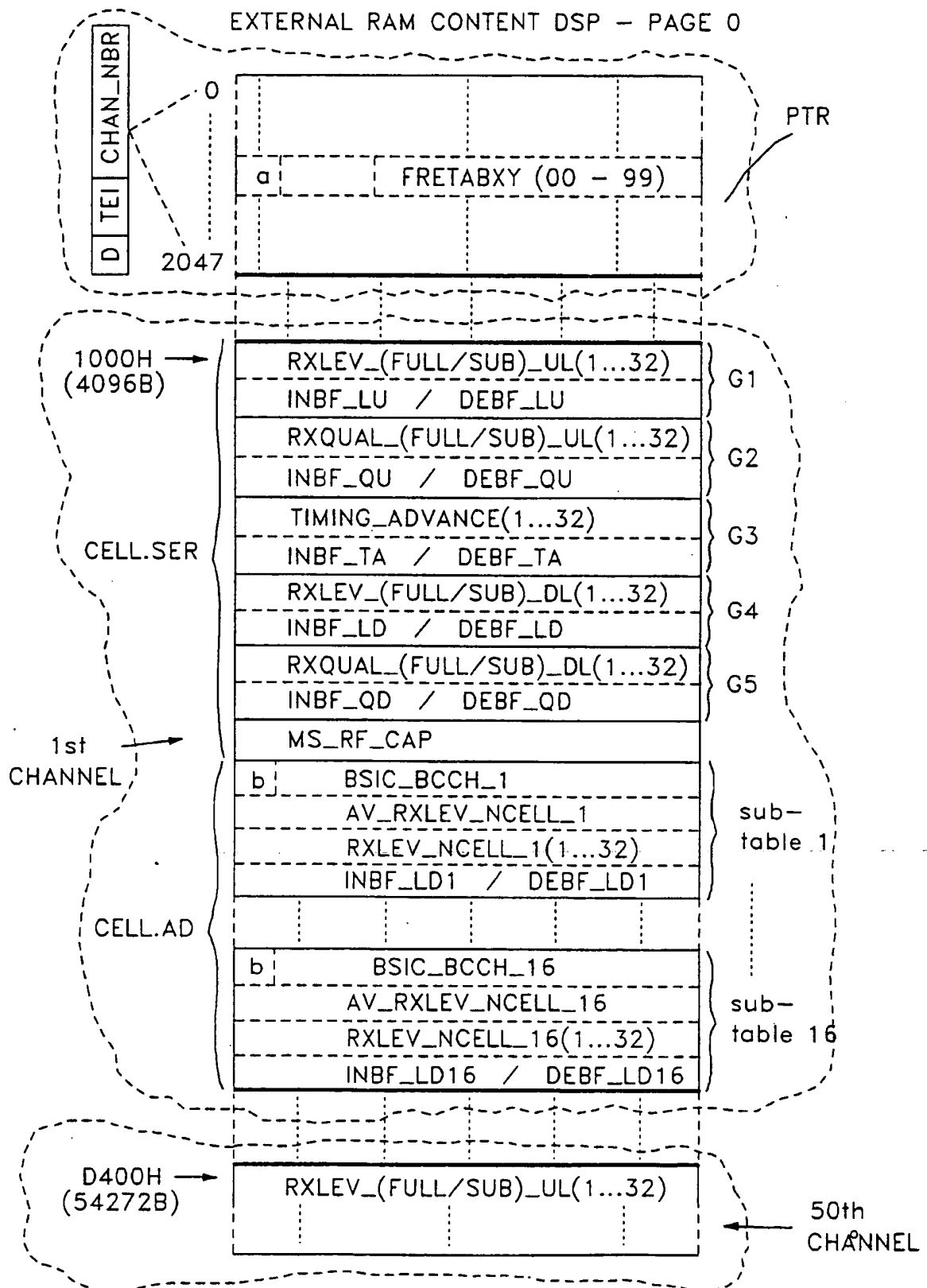


FIG. 8

8/14

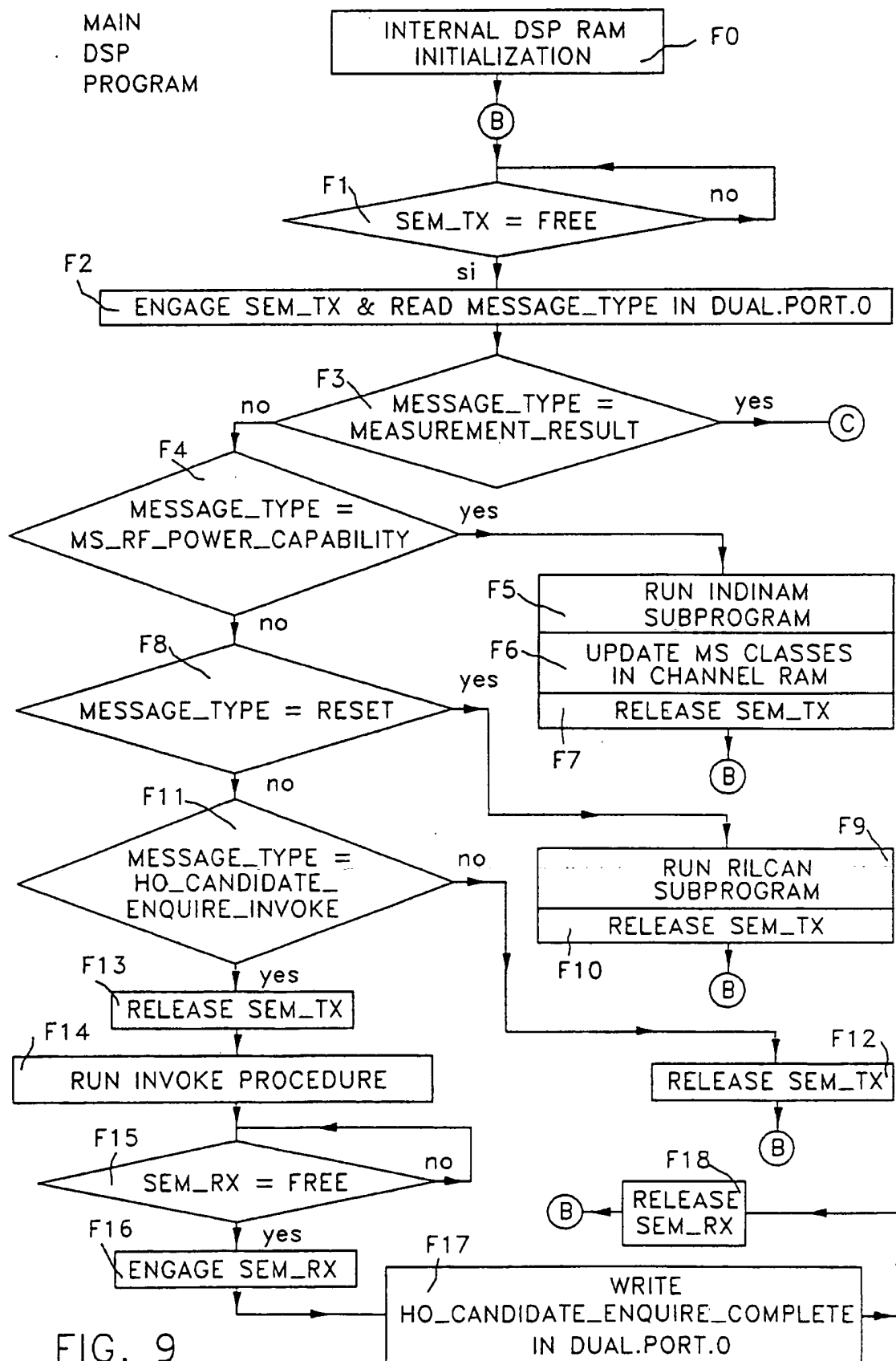


FIG. 9

9/14

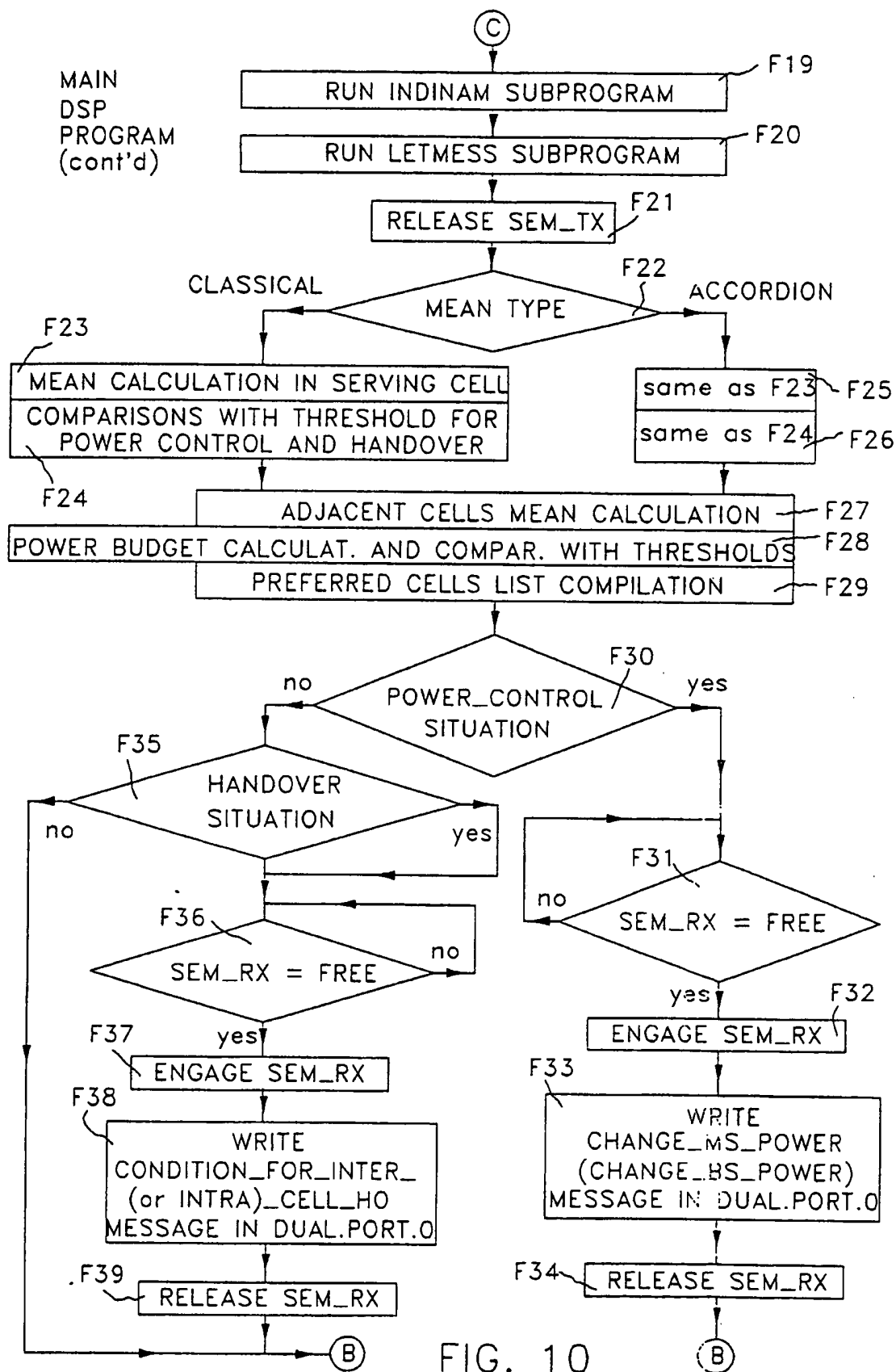


FIG. 10

10/14

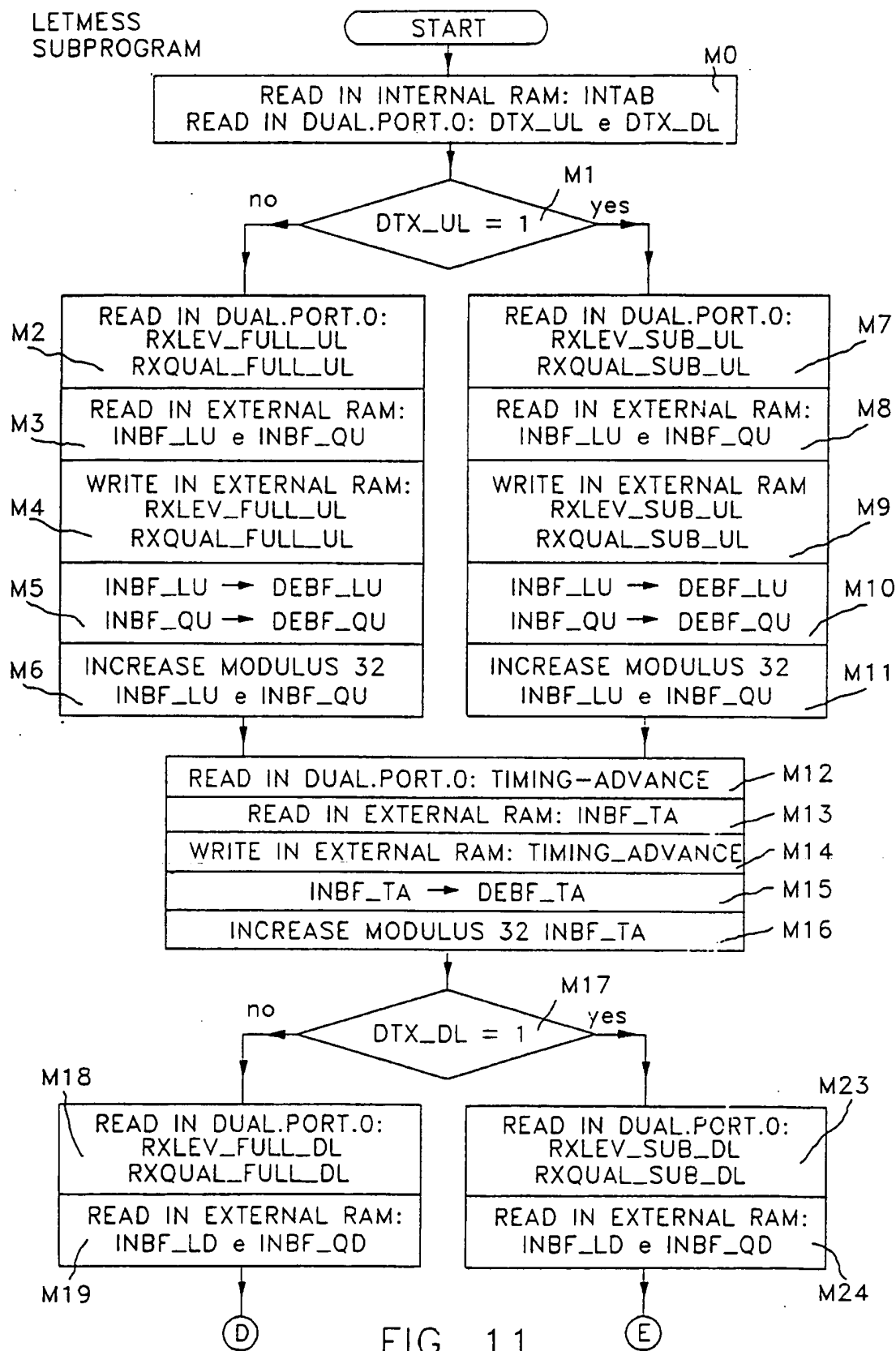
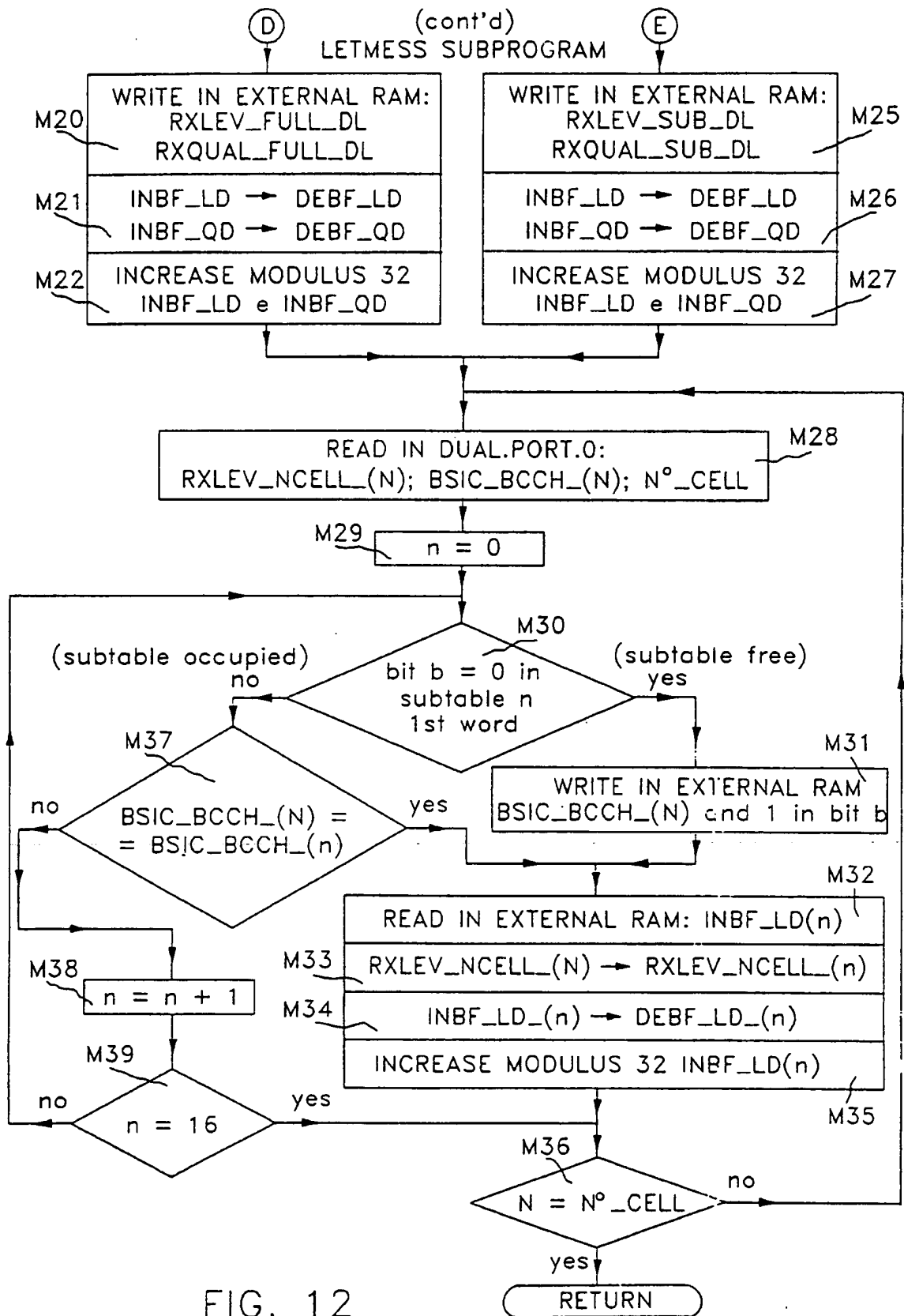


FIG. 11



11/14



12/14

MAIN  
DSP  
PROGRAM  
(PHASE F0)

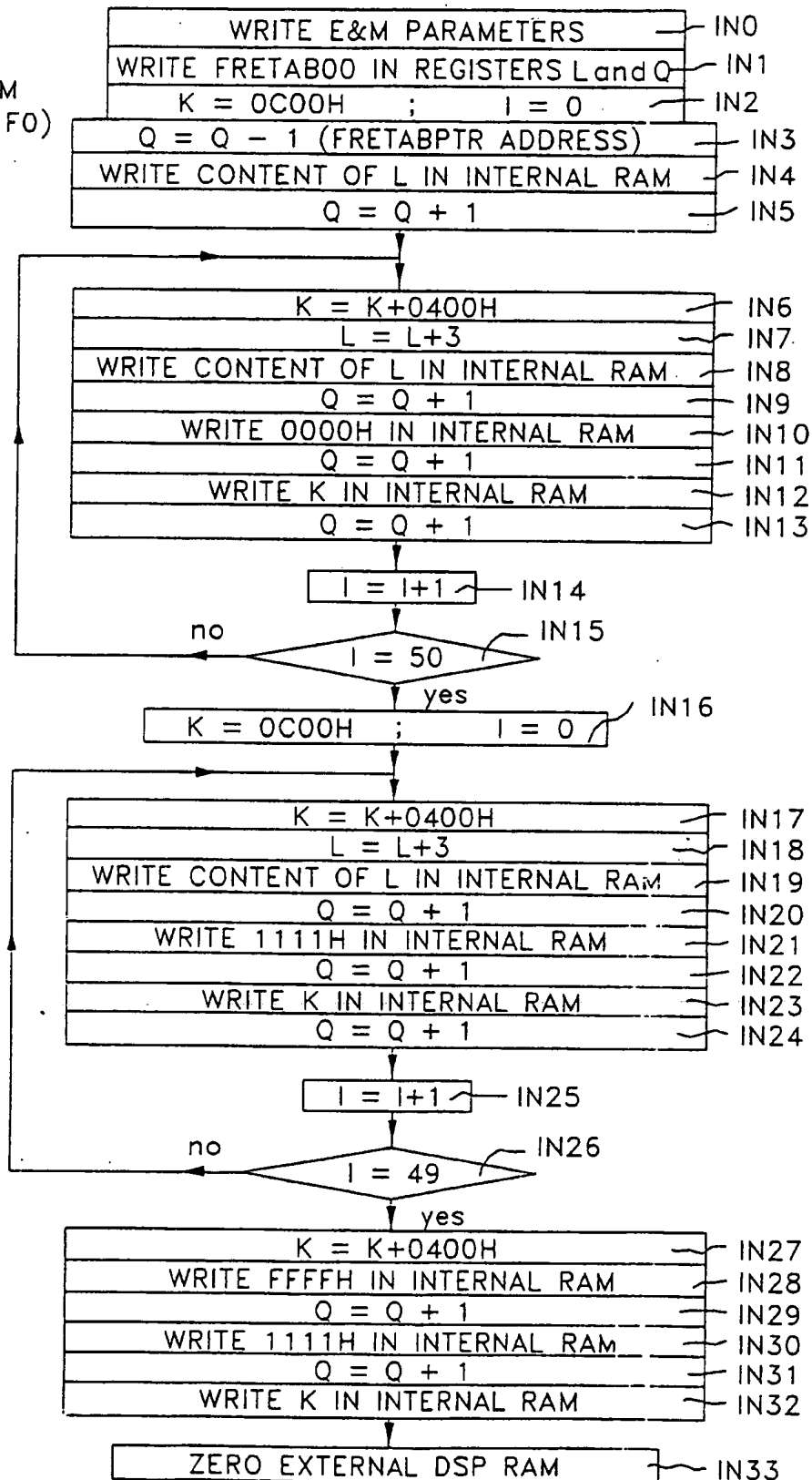
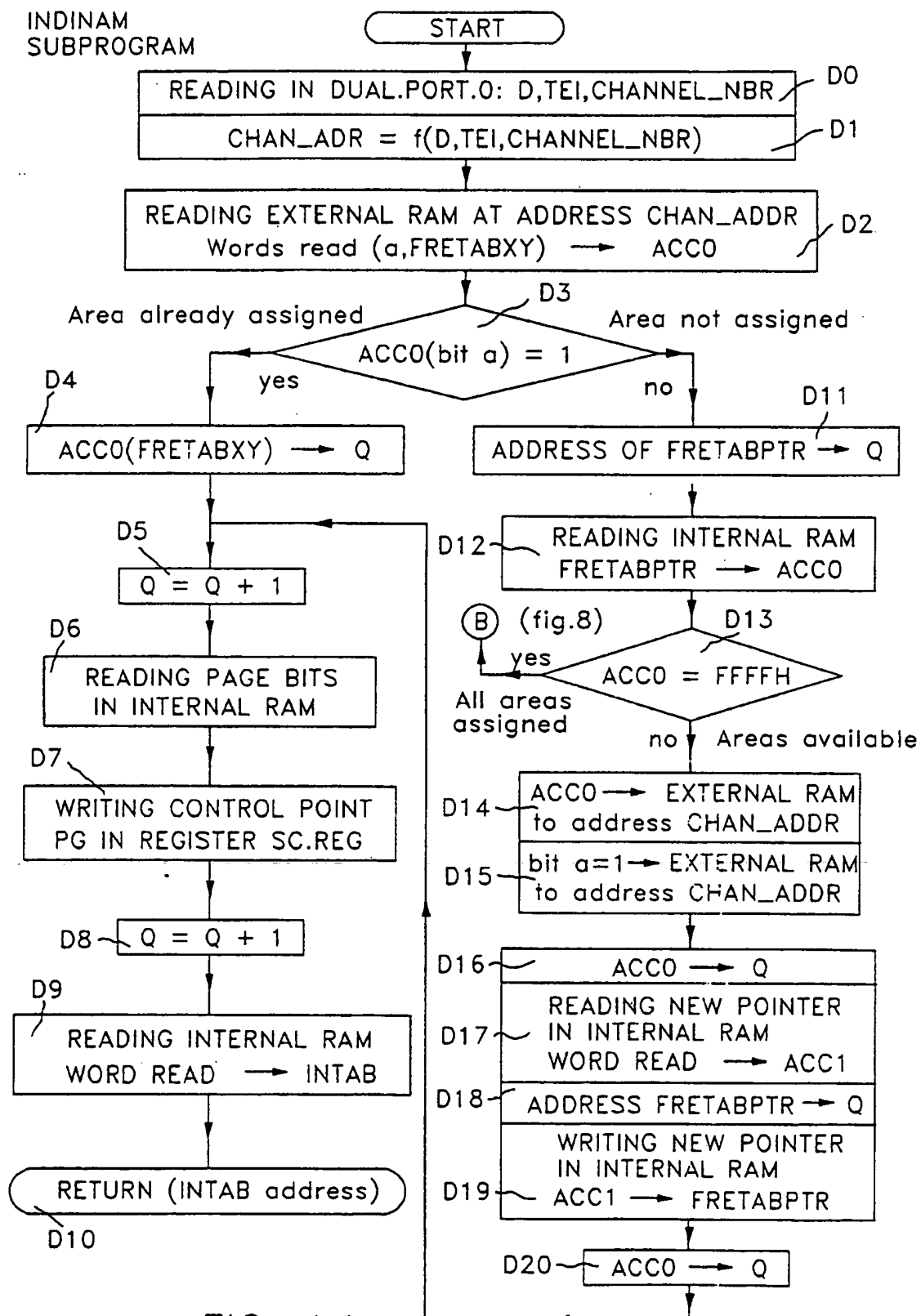


FIG. 13

(B)

13/14



14/14

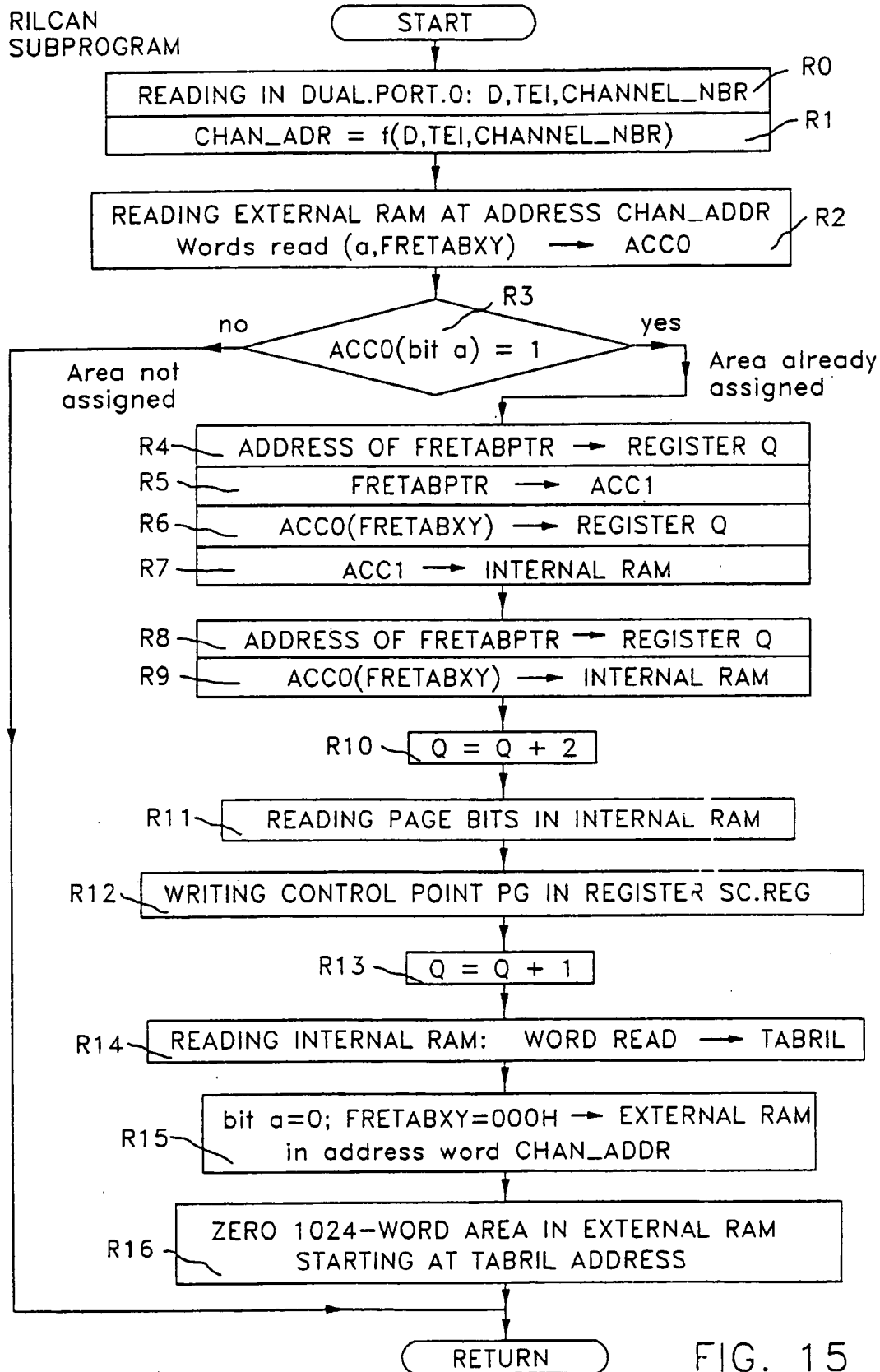


FIG. 15

## INTERNATIONAL SEARCH REPORT

Internat'l Application No  
PCT/EP 94/01854

A. CLASSIFICATION OF SUBJECT MATTER  
IPC 5 H04Q7/04 H04B7/26

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 5 H04Q H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PHILIPS TELECOMMUNICATION REVIEW, vol.50, no.2, August 1992, HILVERSUM NL pages 78 - 83, XP000315529 MCMATHON 'Base station control using DSP techniques' see the whole document -----	1



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

## \* Special categories of cited documents :

- \*A\* document defining the general state of the art which is not considered to be of particular relevance
- \*E\* earlier document but published on or after the international filing date
- \*I\* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- \*O\* document referring to an oral disclosure, use, exhibition or other means
- \*P\* document published prior to the international filing date but later than the priority date claimed

\*T\* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

\*X\* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

\*Y\* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

\*&\* document member of the same patent family

Date of the actual completion of the international search

6 October 1994

Date of mailing of the international search report

17. 10. 94

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